Si Nanowire FET Modeling and Technology

November 8, 2010

@ Peking University

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Tokyo Inst. Tech.

First Computer Eniac: made of huge number of vacuum tubes 1946

Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

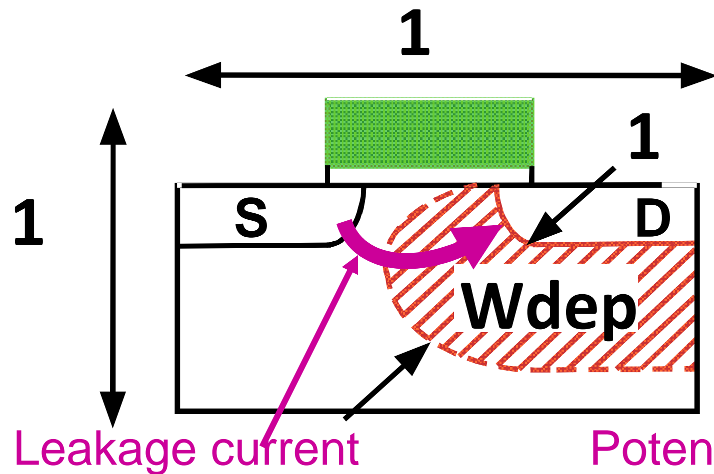
Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption

Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

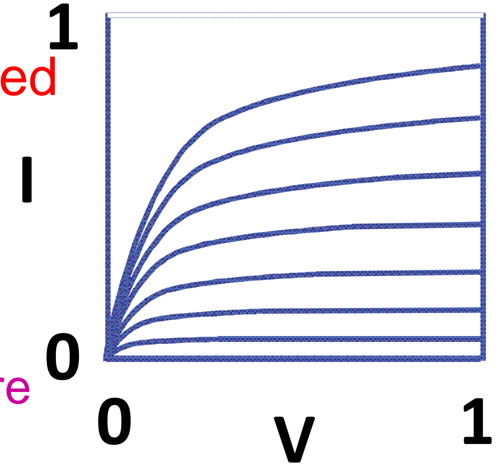
In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

Scaling Method: by R. Dennard in 1974



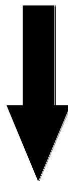
Wdep: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed
Otherwise, large leakage between S and D



Leakage current

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

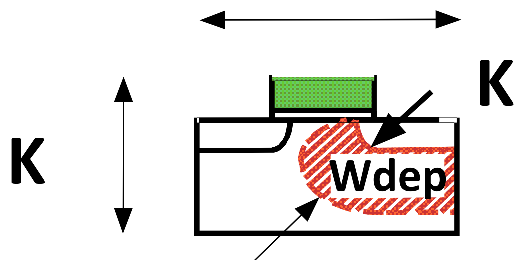


K=0.7 for example

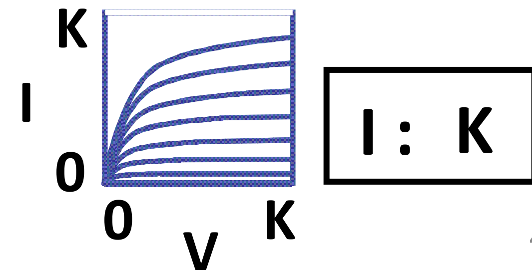
X , Y , Z : K, V : K, Na : 1/K

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

→ Good scaled I-V characteristics



Wdep $\propto \sqrt{V/Na}$
: K



I : K

Downscaling merit: Beautiful!

Geometry & Supply voltage	L_g, W_g T_{ox}, V_{dd}	K	**Scaling K : K=0.7 for example**
Drive current in saturation	I_d	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ C_o: gate C per unit area → $W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1}(V_g - V_{th}) = KK^{-1}K = K$
I_d per unit W_g	$I_d/\mu m$	1	I_d per unit $W_g = I_d / W_g = 1$
Gate capacitance	C_g	K	$C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox}$ → $KK/K = K$
Switching speed	τ	K	$\tau = C_g V_{dd} / I_d$ → $KK/K = K$
Clock frequency	f	1/K	$f = 1/\tau = 1/K$
Chip area	A_{chip}	α	α: Scaling factor → **In the past, $\alpha > 1$ for most cases**
Integration (# of Tr)	N	α/K^2	N → α/K^2 **$= 1/K^2$, when $\alpha = 1$**
Power per chip	P	α	$fNCV^2/2$ → $K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha$ **= 1, when $\alpha = 1$**

k= 0.7 and α =1	k= 0.7^2 =0.5 and α =1
Single MOFET Vdd → 0.7 Lg → 0.7 Id → 0.7 Cg → 0.7 P (Power)/Clock → $0.7^3 = 0.34$ τ (Switching time) → 0.7	Vdd → 0.5 Lg → 0.5 Id → 0.5 Cg → 0.5 P (Power)/Clock → $0.5^3 = 0.125$ τ (Switching time) → 0.5
Chip N (# of Tr) → $1/0.7^2 = 2$ f (Clock) → $1/0.7 = 1.4$ P (Power) → 1	N (# of Tr) → $1/0.5^2 = 4$ f (Clock) → $1/0.5 = 2$ P (Power) → 1

Integrated Circuits Technologies are still very important for Green or power saving!

1. Green by Integrated Circuits

   Power saving by Microprocessor control for all the human systems

2. Green of Integrated Circuits

   Power saving of Integrated Circuits by Down Scaling of MOSFETs in PC, Data Center, Router, etc.

Down scaling is the most effective way of Power saving.

It has been always discussed about the limit of downscaling, but the down scaling of MOSFETs is still possible for another 10 or 20 years!

3 important technological items for DS.

1. Thinning of high-k beyond 0.5 nm
2. Metal S/D
3. Si-Nanowire FET

Question:

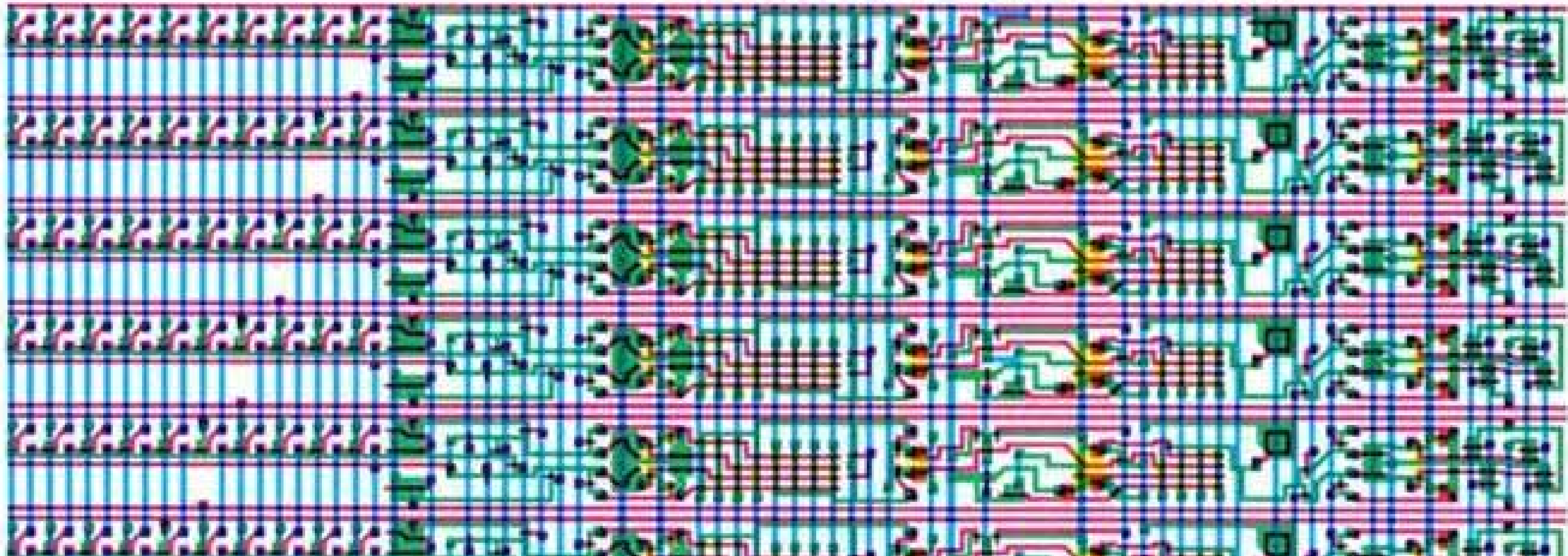
How far we can go with downscaling?

Many people wanted to say about the limit. Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970's	1μm:	SCE
Early 1980's	0.5μm:	S/D resistance
Early 1980's	0.25μm:	Direct-tunneling of gate SiO_2
Late 1980's	0.1μm:	'0.1μm brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

Historically, many predictions of the limit of downsizing.

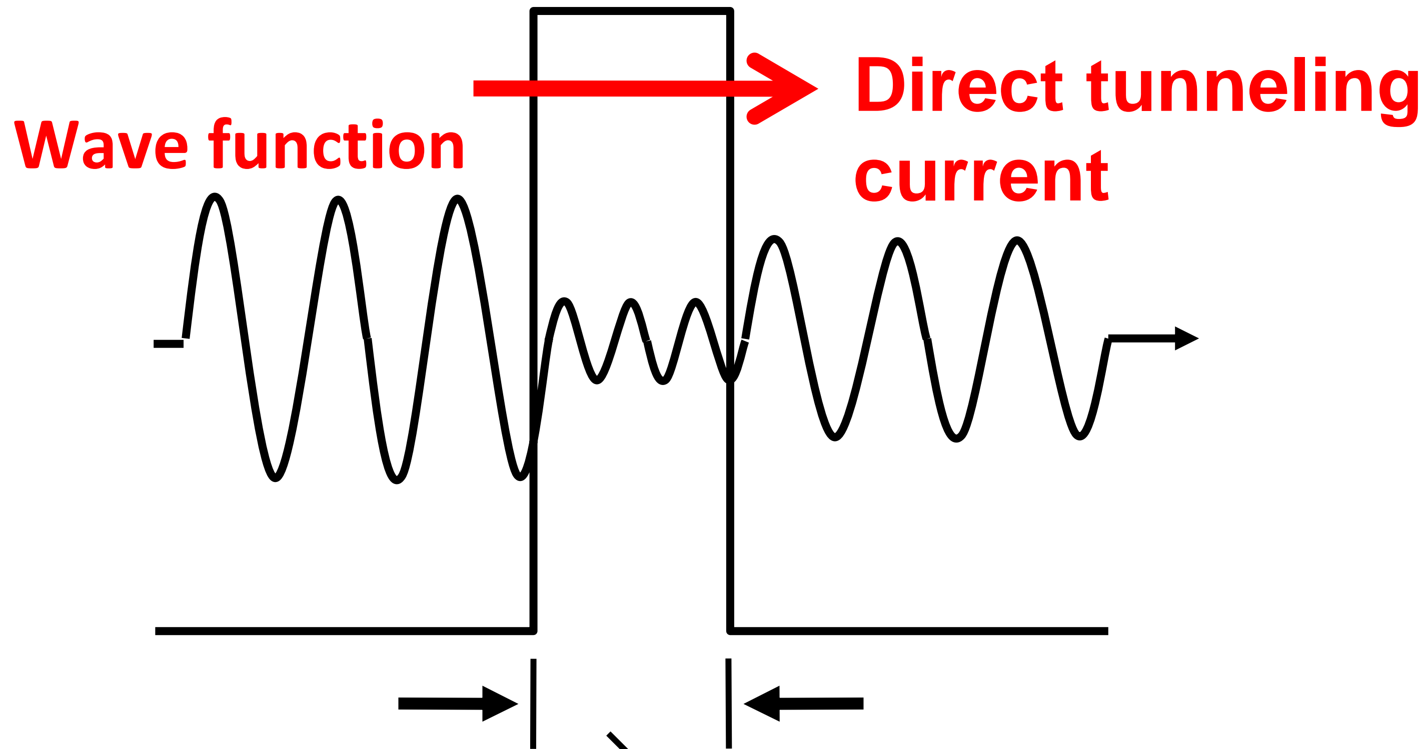
VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.

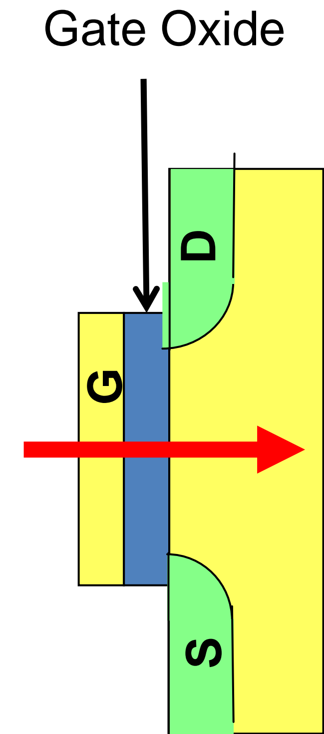


VLSI textbook

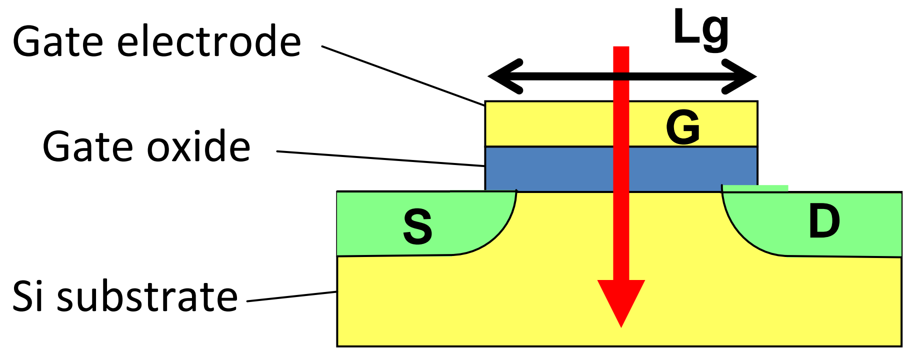
Finally, there appears to be a fundamental limit [10] of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide ..... begin to make the devices of smaller dimension unworkable.

Direct-tunneling effect





Direct tunneling leakage current start to flow when the thickness is 3 nm.



MOSFETs with 1.5 nm gate oxide

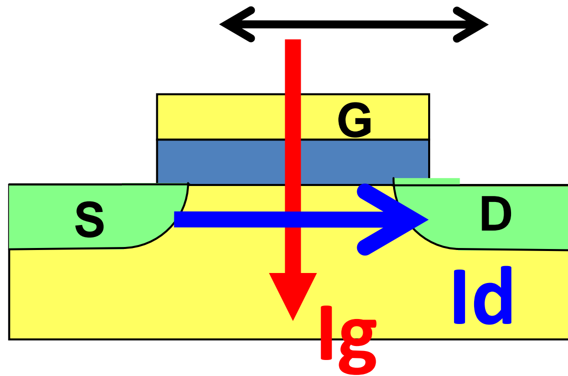
Direct tunneling leakage was found to be OK! In 1994!

Lg = 10 μm

Lg = 5 μm

Lg = 1.0 μm

Lg = 0.1μm



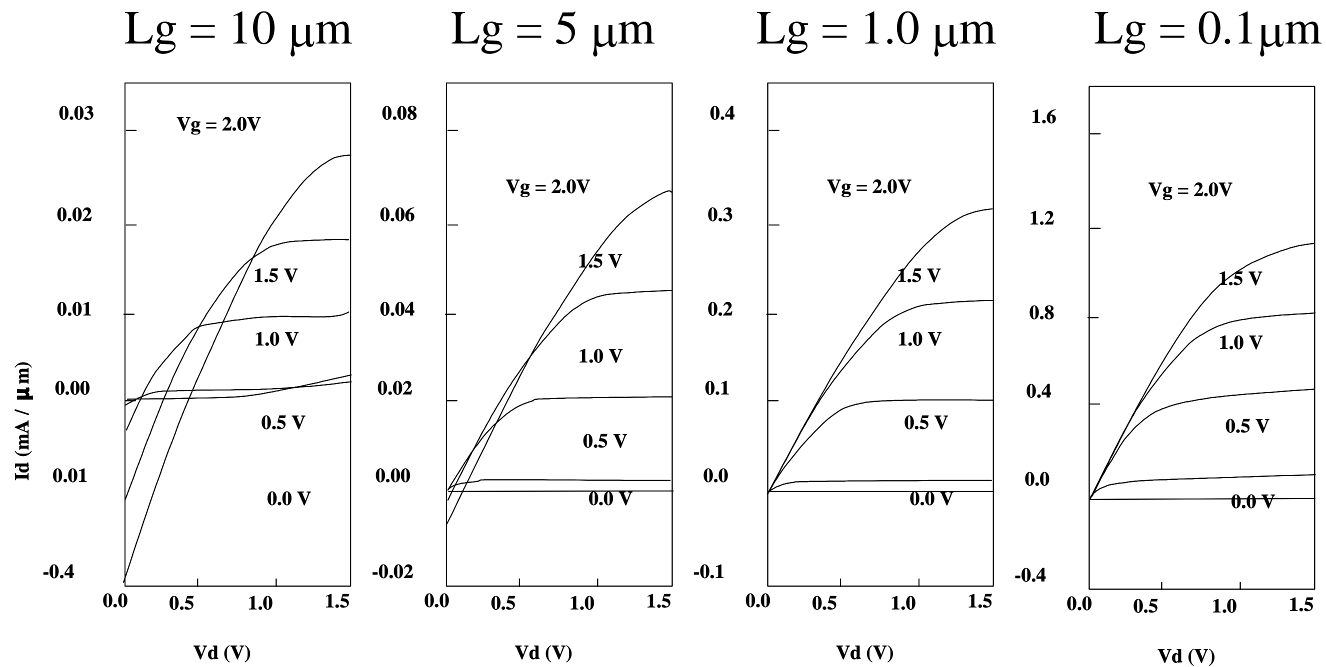
Gate leakage: Ig $\propto$ Gate Area $\propto$ Gate length (Lg)

Drain current: Id $\propto$ 1/Gate length (Lg)

Lg → small,

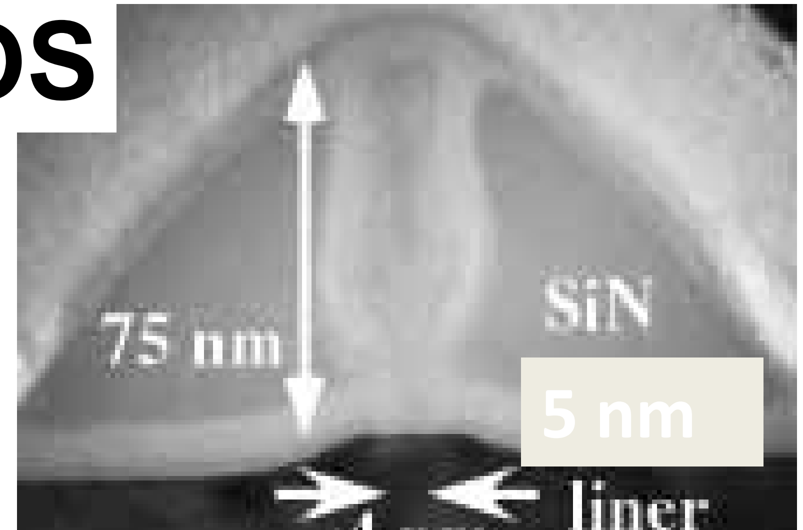
Then, Ig → small, Id → large, Thus, Ig/Id → very small

Id

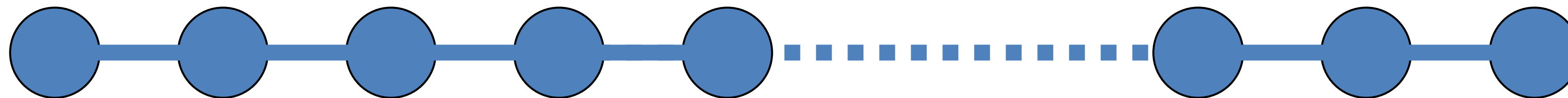


5 nm gate length CMOS

Is a Real Nano Device!!

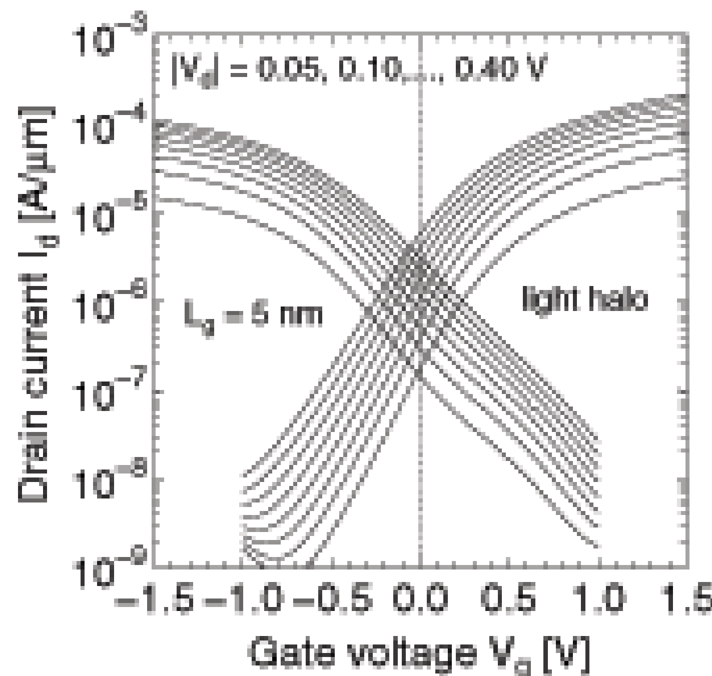


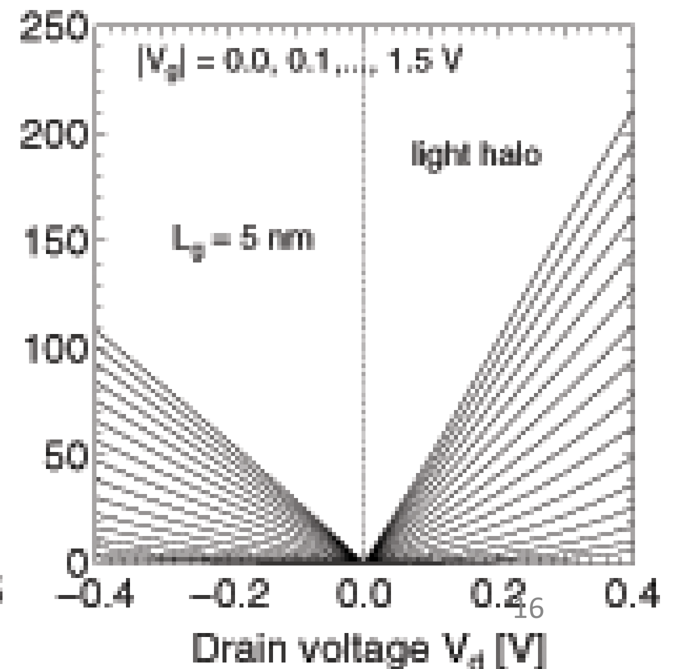
Length of 18 Si atoms



H. Wakabayashi
et.al, NEC

IEDM, 2003

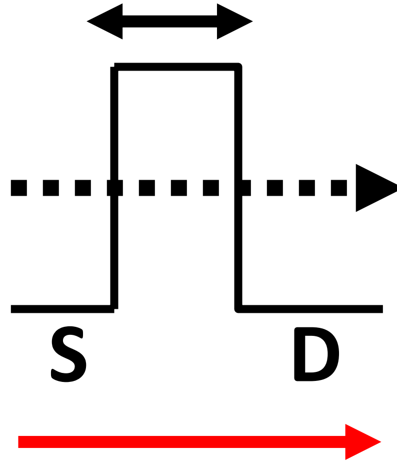




Predicted limit now

Tunneling distance

3 nm



MOSFET operation

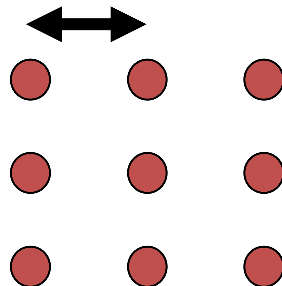
Lg = 3 nm?

Below this, no one knows future!

Ultimate Limit

Atom distance

0.3 nm



ITRS expect Lg less than 10nm

2009 ITRS Technology Trend: MPU gate length

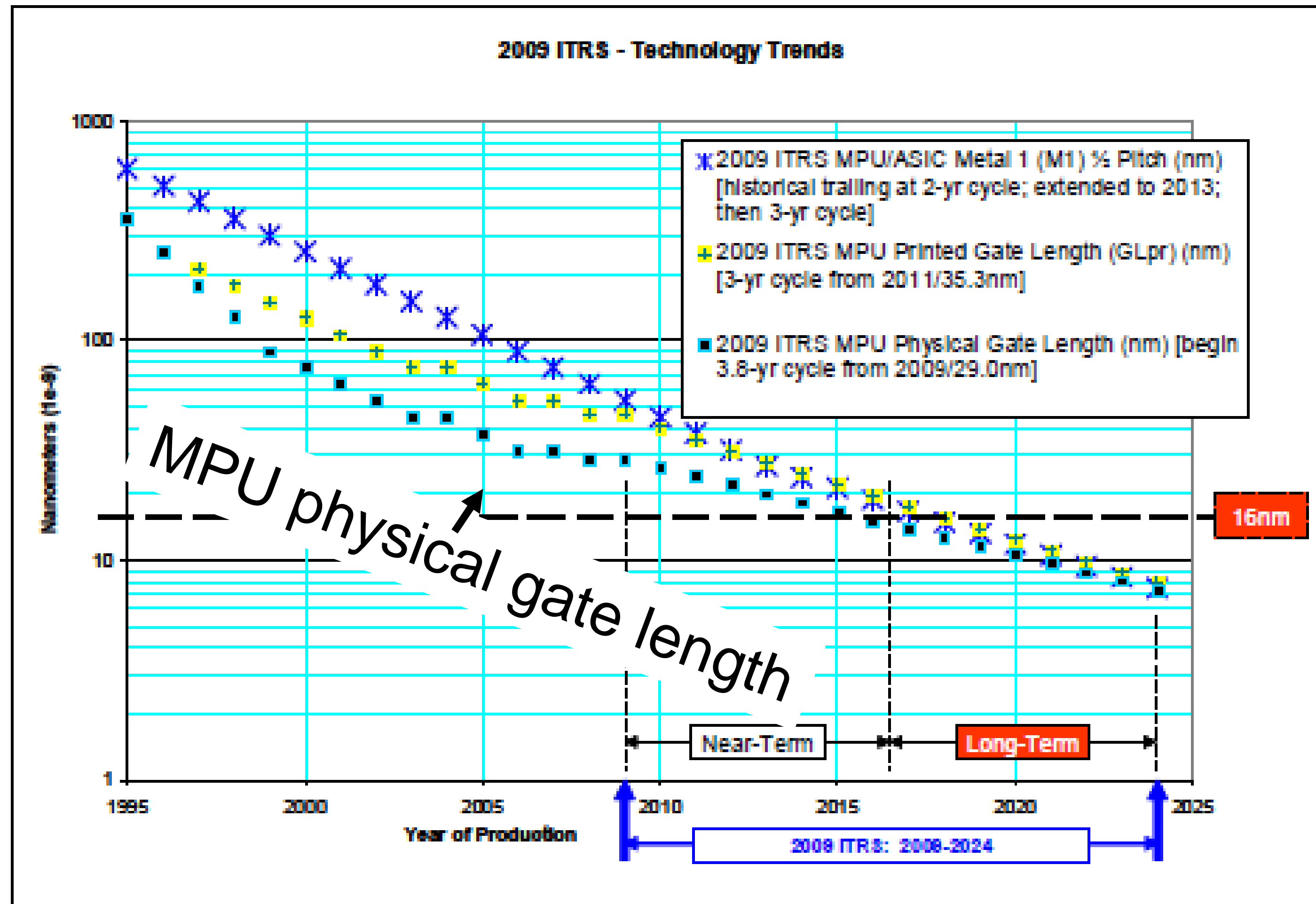


Figure 8b 2009 ITRS—MPU/high-performance ASIC Half Pitch and Gate Length Trends

ITRS

How far can we go?

Past

0.7 times per 3 years

In 40 years: 15 generations,
Size 1/200, Area 1/40,000

1973年

Now

8μm → 6μm → 4μm → 3μm → 2μm → 1.2μm → 0.8μm → 0.5μm

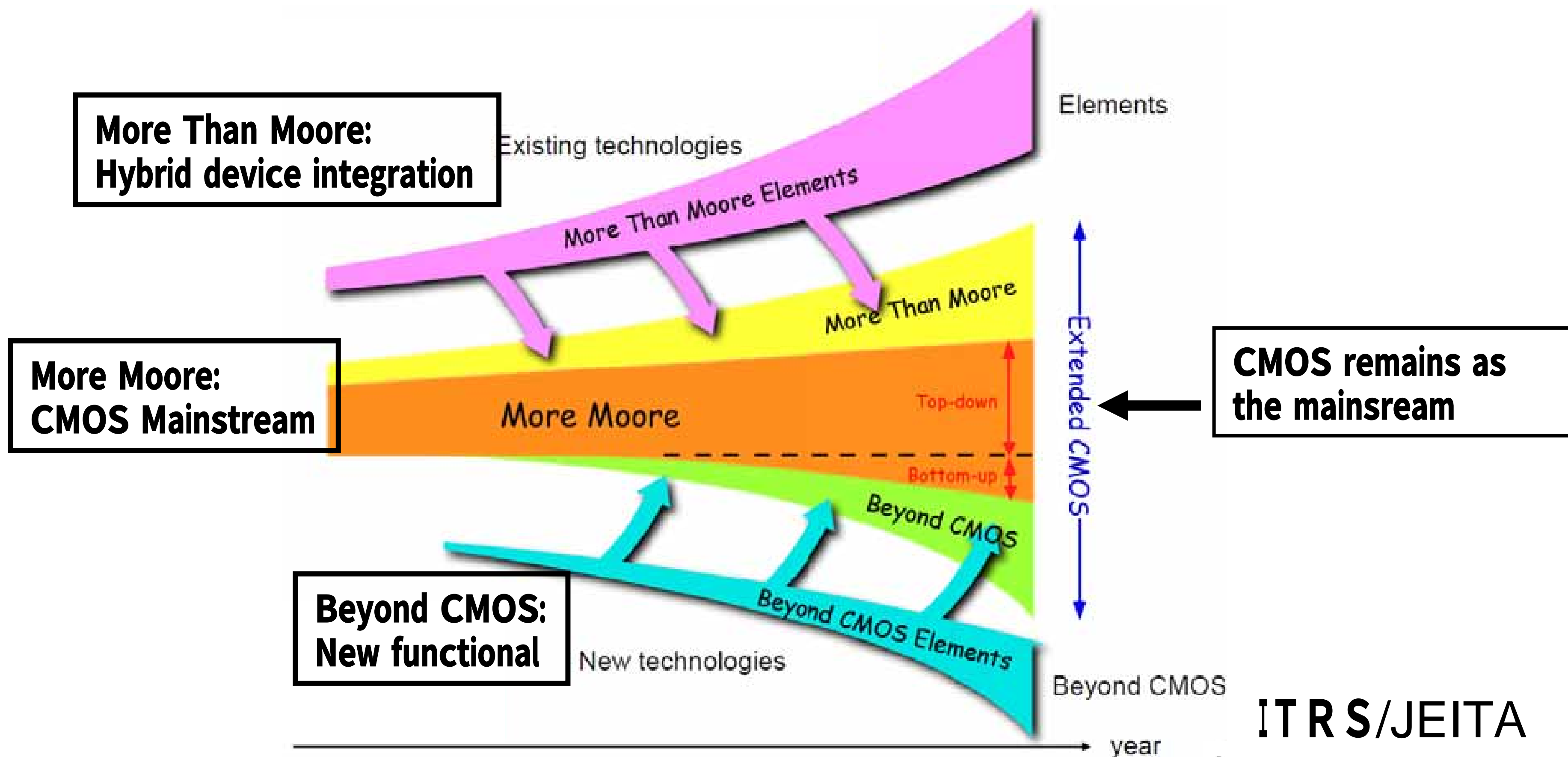
→ 0.35μm → 0.25μm → 180nm → 130nm → 90nm → 65nm → 45nm

Future

→ 32nm → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

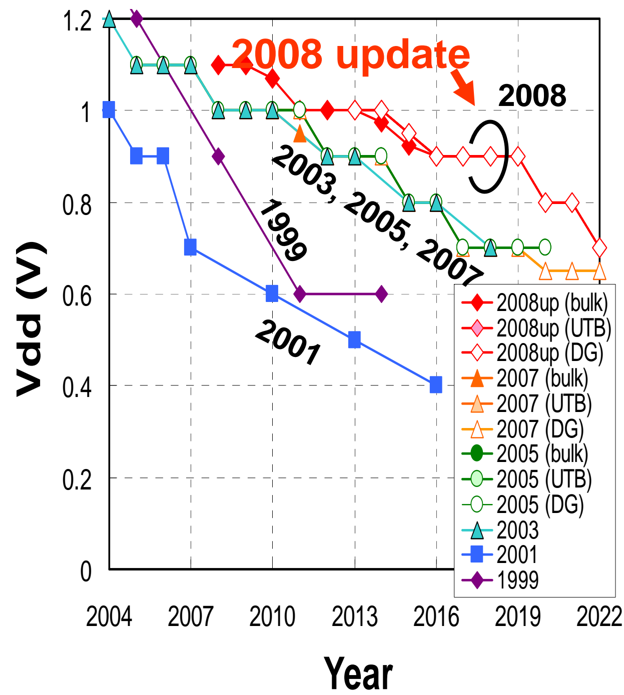
- **At least 5,6 generations, for 15 ~ 20 years**
- **Hopefully 8 generations, for 30 years**

CMOS scaling is the mainstream

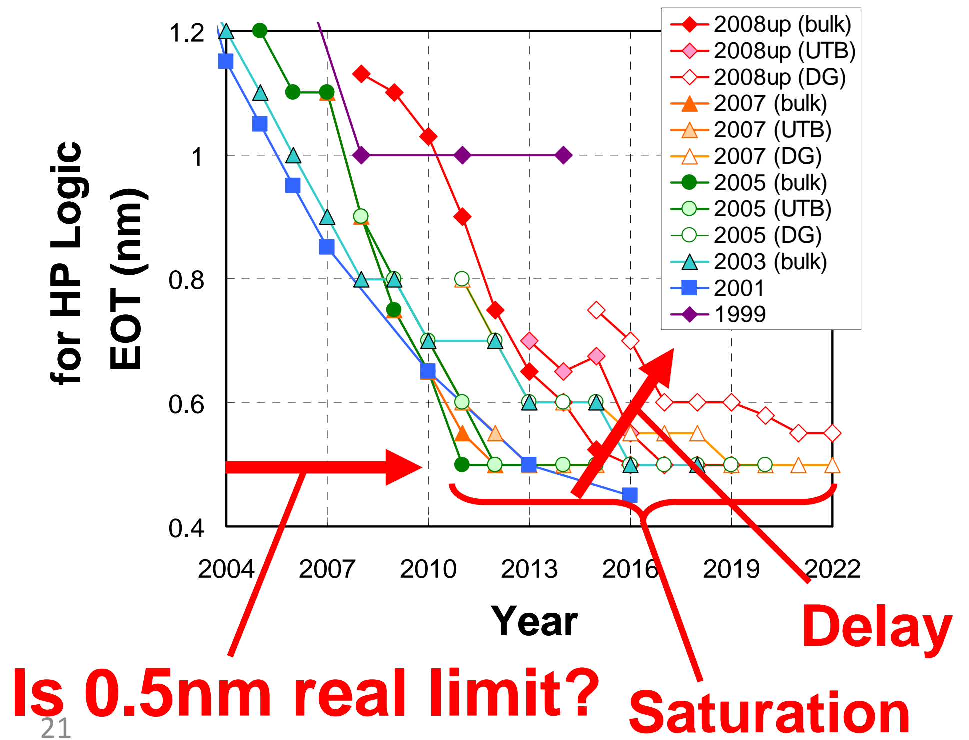


ITRS

Vdd stay high



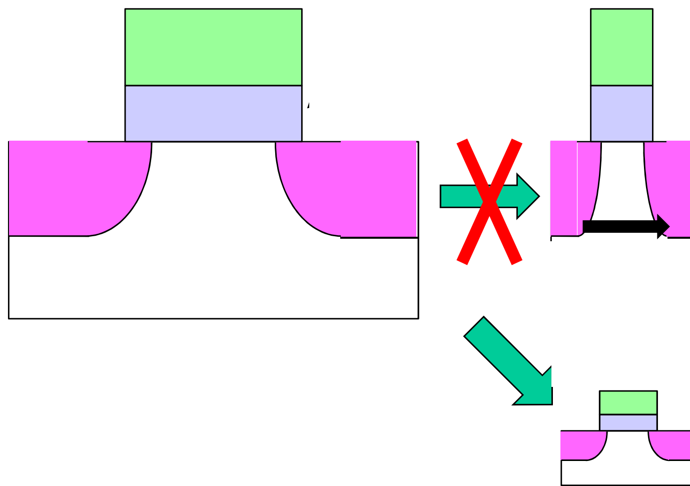
ITRS EOT limit = 0.5 nm?



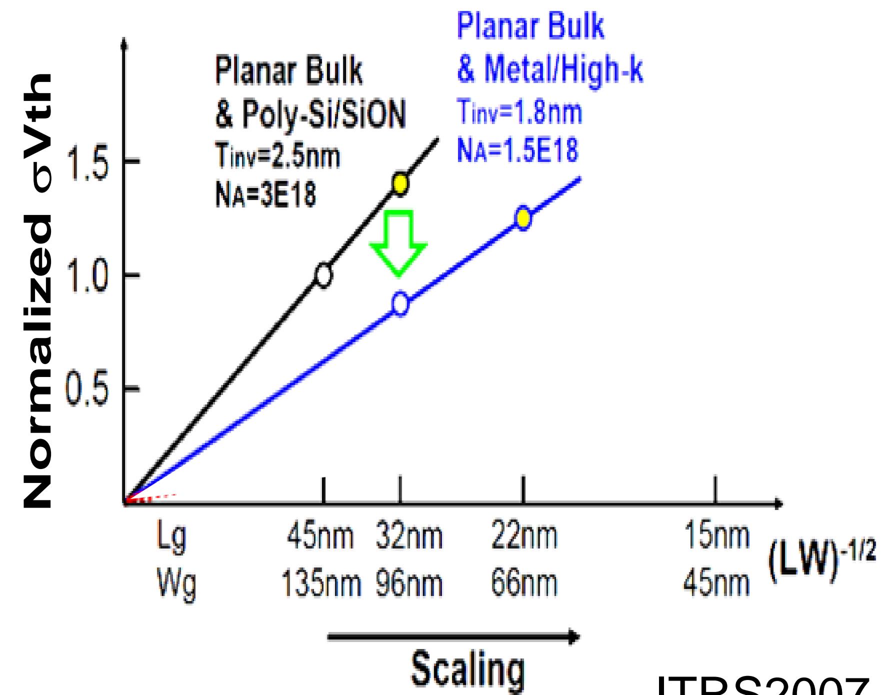
Scaling of high beyond 0.5 nm is important

Power of FET $= CV^2/2 \propto D^3$ $(=L^3)$

Problems
→SCE
→Variation in Vth
→Increase in Off-leakage current

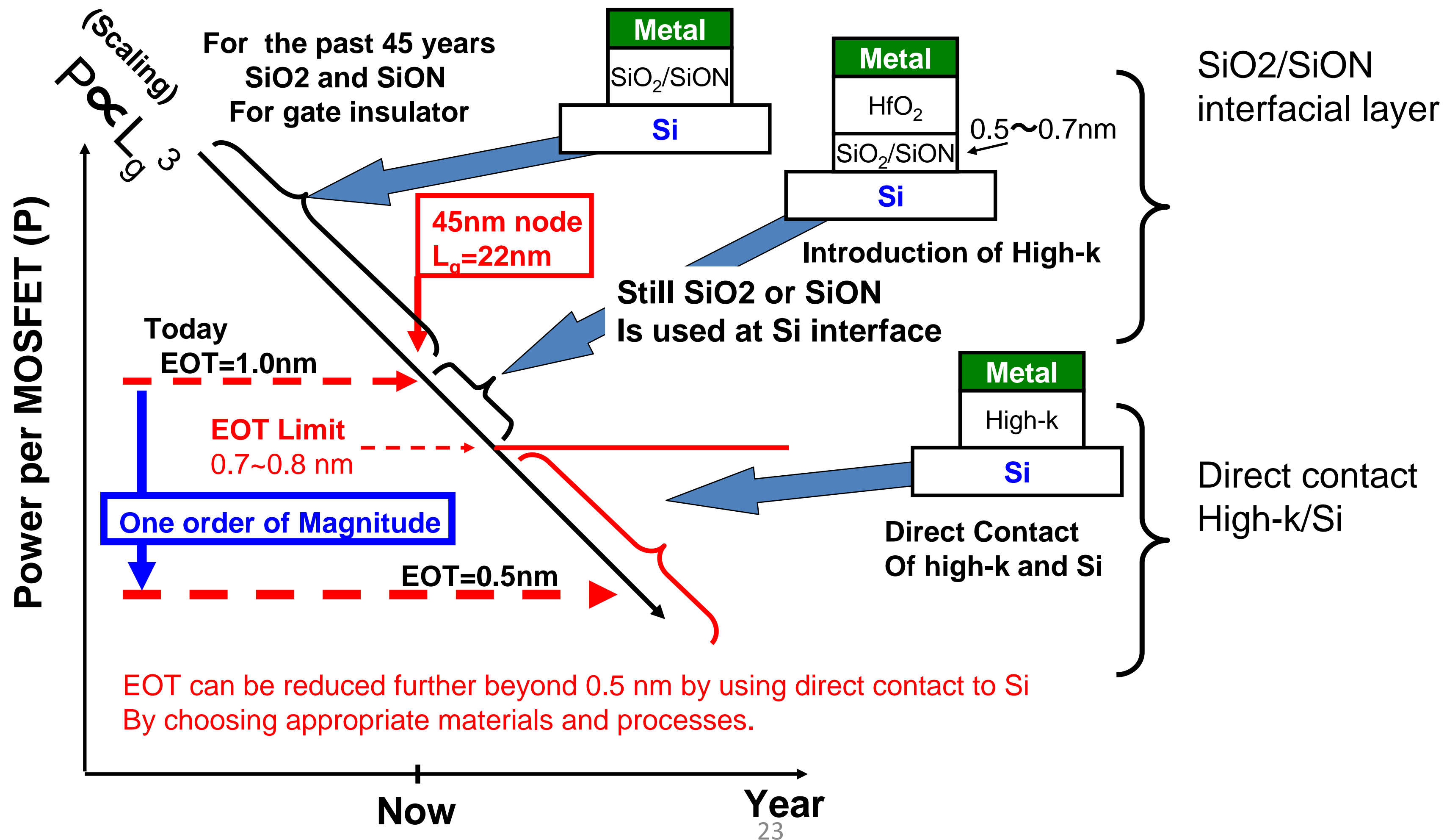


Solution

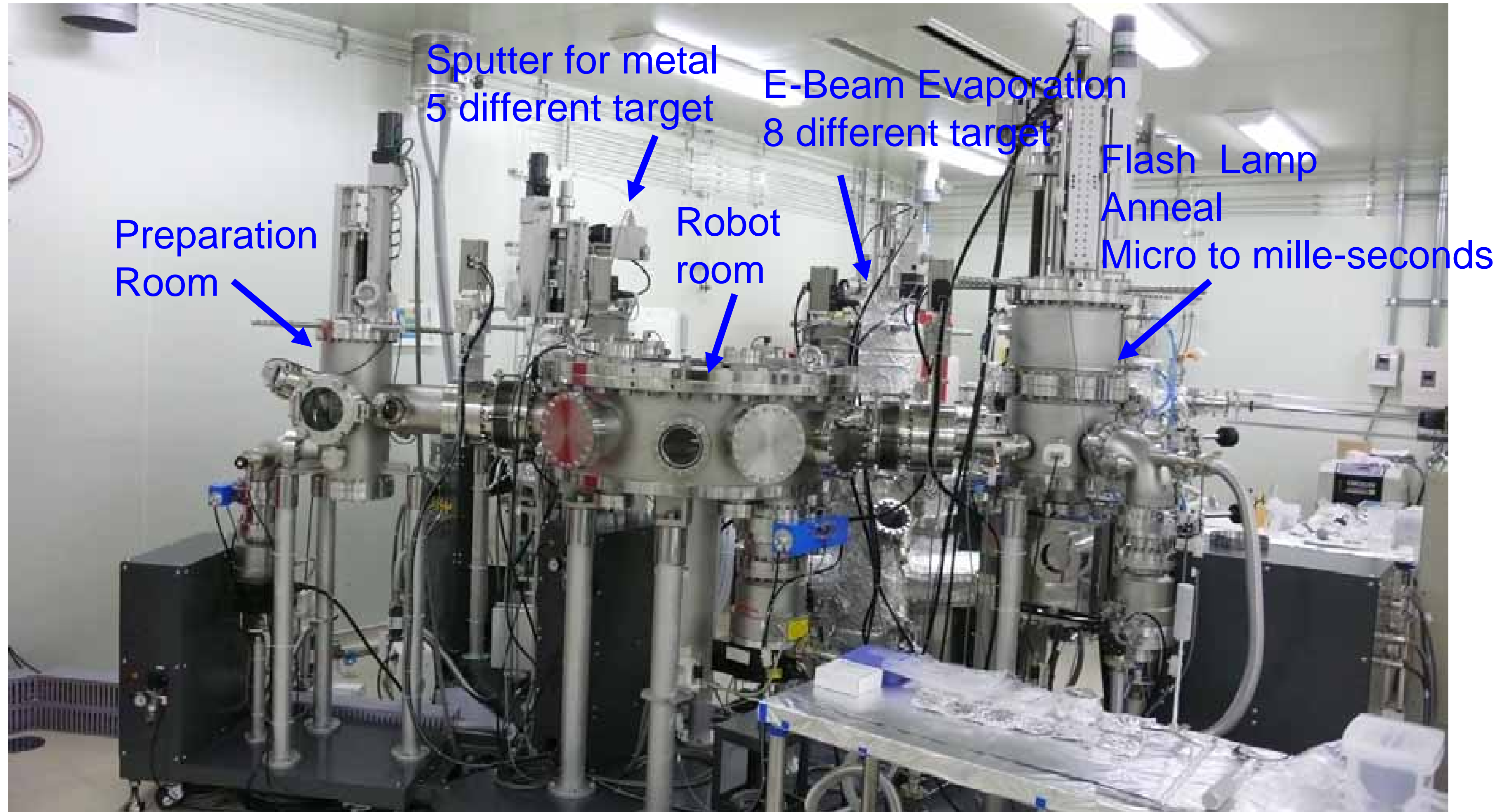


ITRS2007

Direct contact of high-k to Si

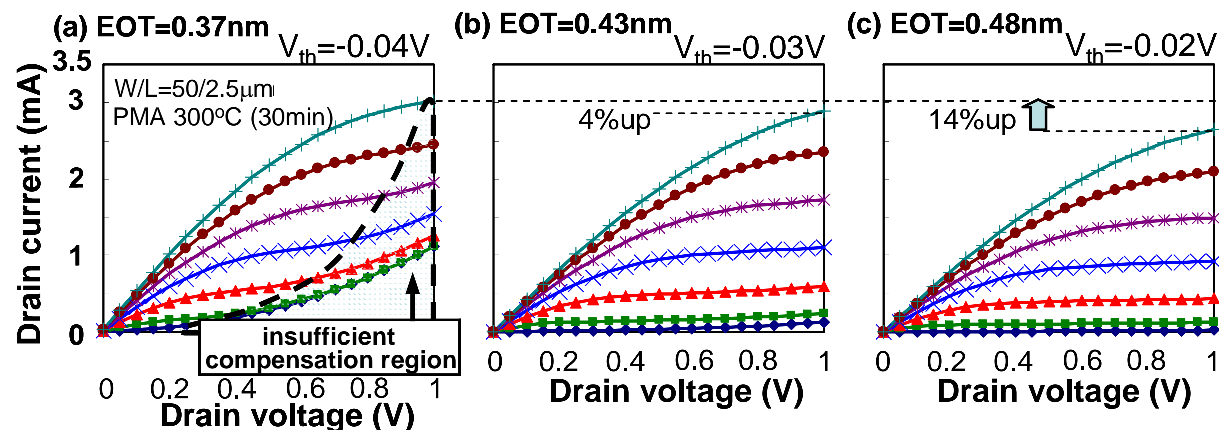


Cluster tool for high-k thin film deposition

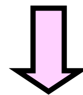


Challenge to EOT~0.3nm

EOT<0.5nm with Gain in Drive Current



14% of I_d increase is observed even at saturation region

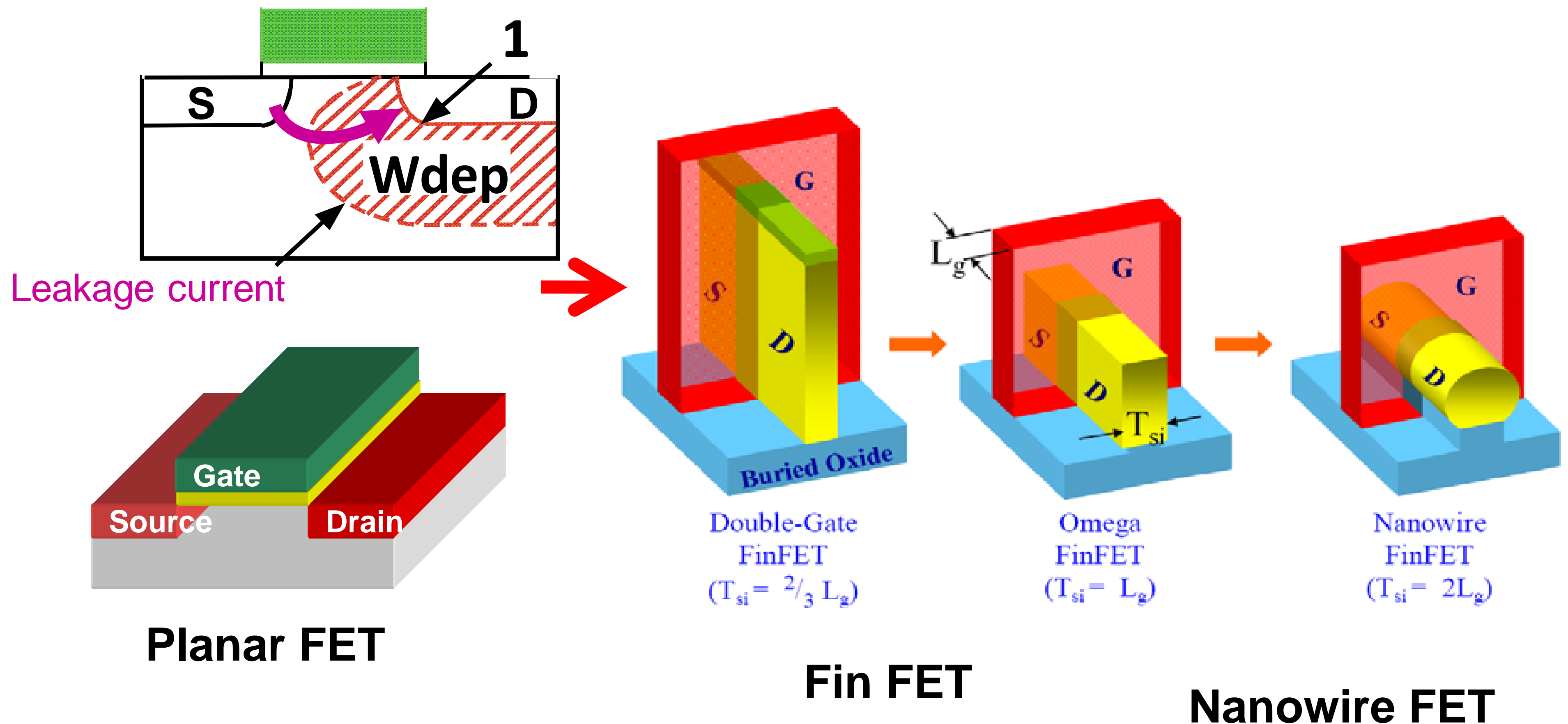


EOT below 0.4nm is still useful for scaling

Si Nanowire FET

Because of off-leakage control,

Planar → Fin → Nanowire



Nanowire FET

First Year of IC Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
Device Structures																
Planar bulk																
FDSOI																
Multiple Gate																

Nanowire FET

Multiple Gate (Fin)FET

ITRS 2009

Bulk → Fin → Nanowire

Scaling Pathways

w and w/o 3rd gate ?

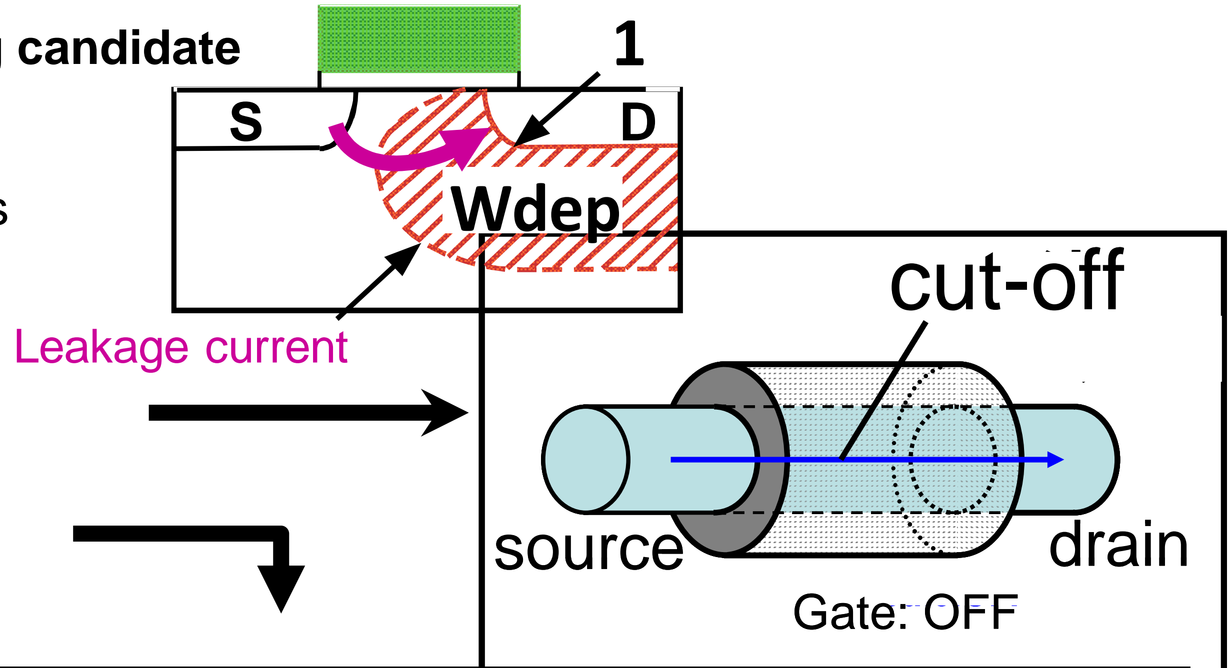
Bulk or SOI

Fin

Si Nanowire

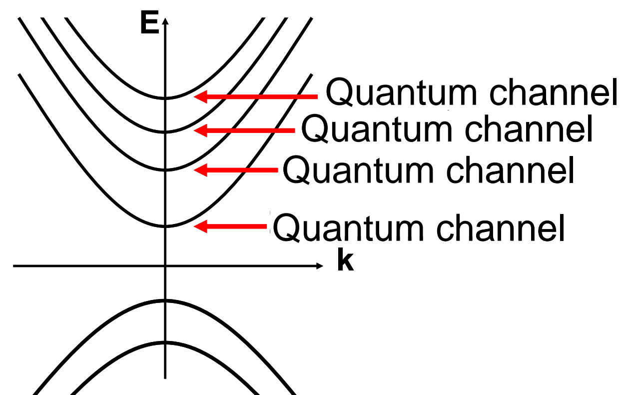
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process
2. Good controllability of I_{OFF}
3. High drive current

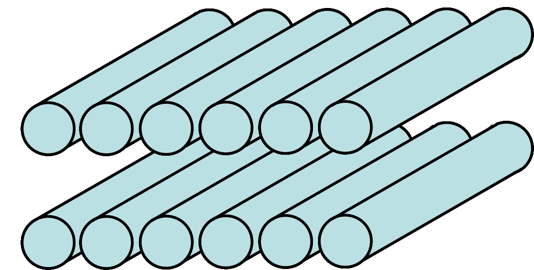


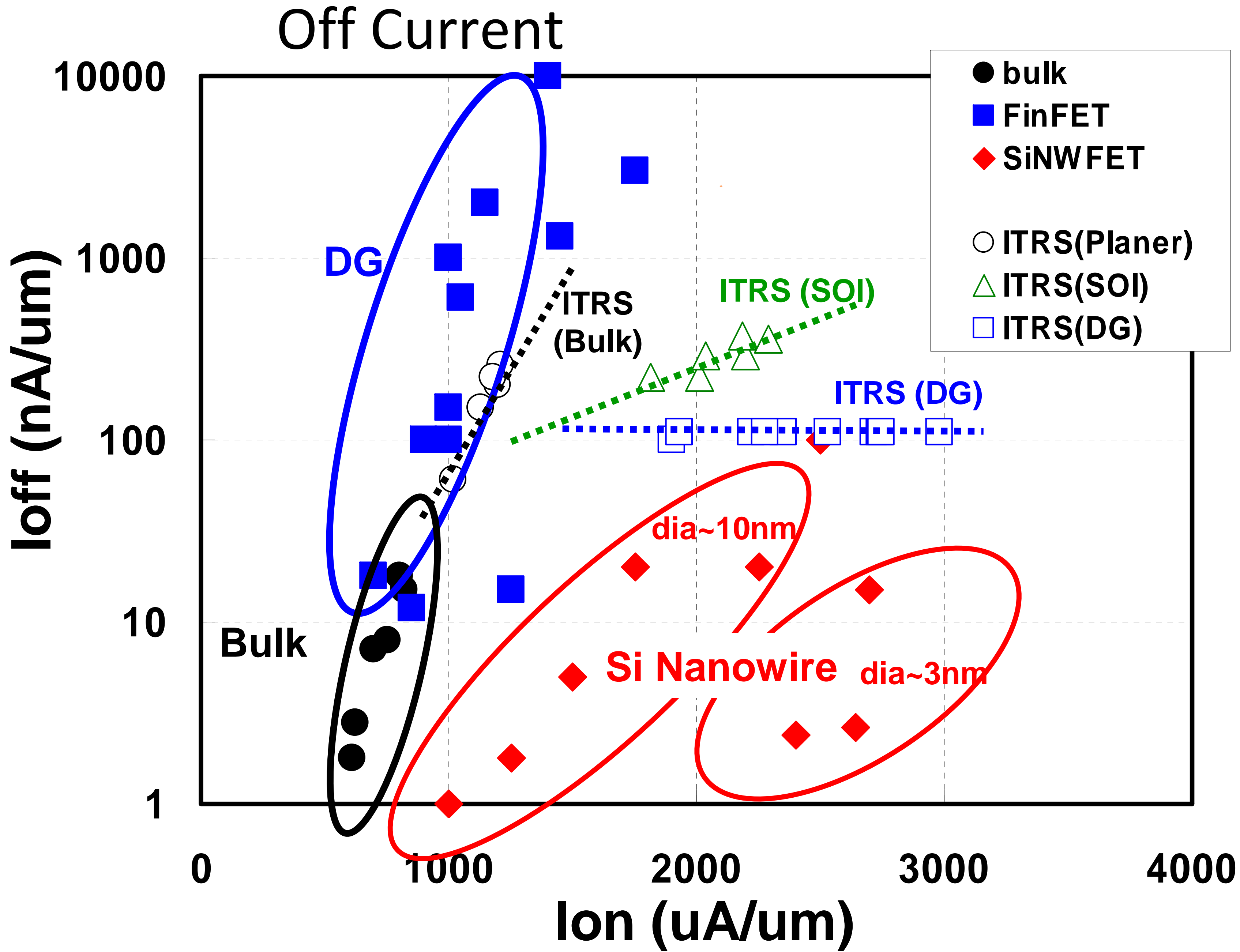
1D ballistic conduction

Multi quantum Channel



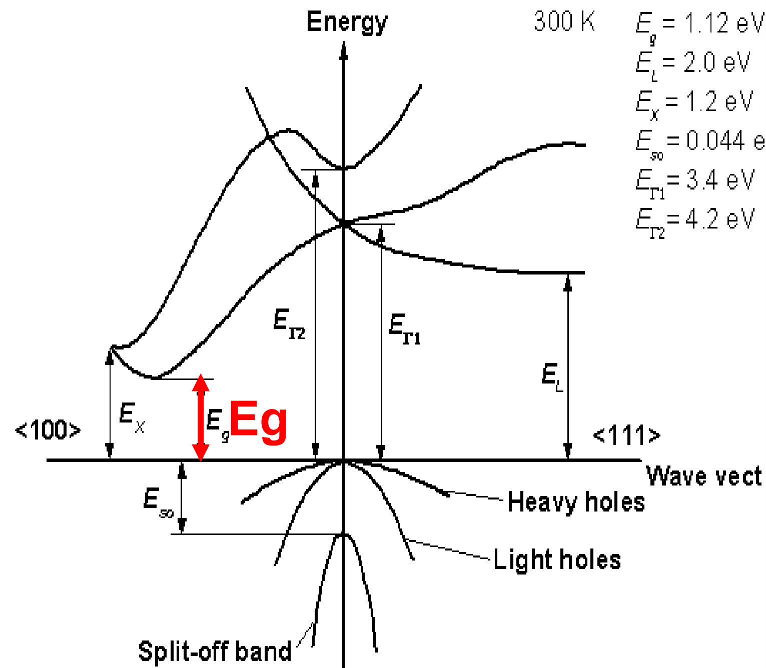
High integration of wires



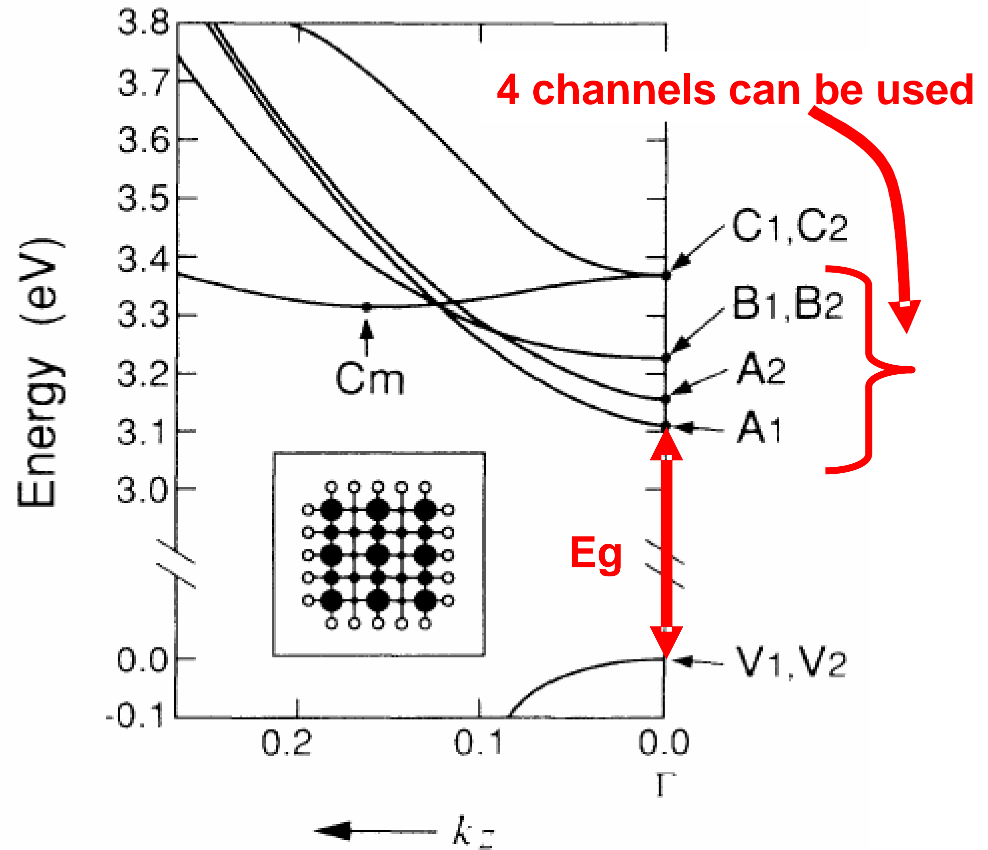

Off Current
10000
1000
100
10
1
0
1000
2000
3000
4000
Ioff (nA/um)
Ion (uA/um)
bulk
FinFET
SiNWFET
ITRS(Planer)
ITRS(SOI)
ITRS(DG)
DG
ITRS
(Bulk)
ITRS (SOI)
ITRS (DG)
dia~10nm
Bulk
Si Nanowire
dia~3nm

Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.



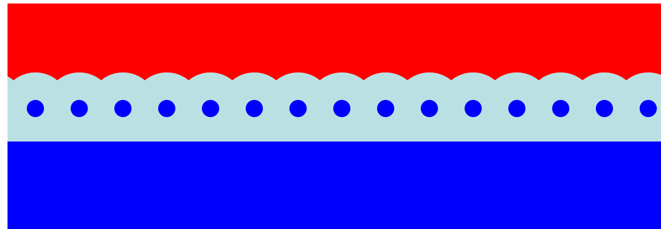
Energy band of Bulk Si



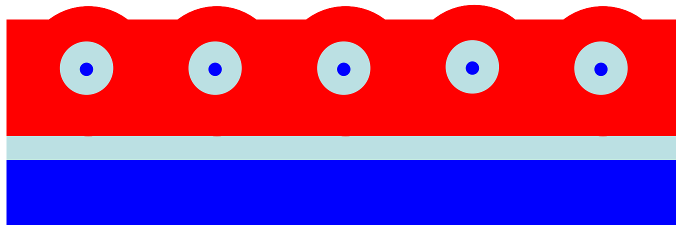
Energy band of 3 x 3 Si wire

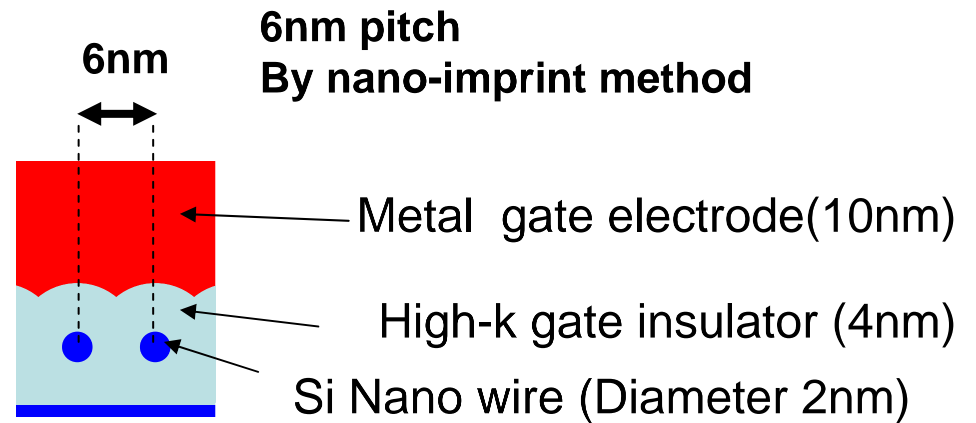
Maximum number of wires per 1 μm

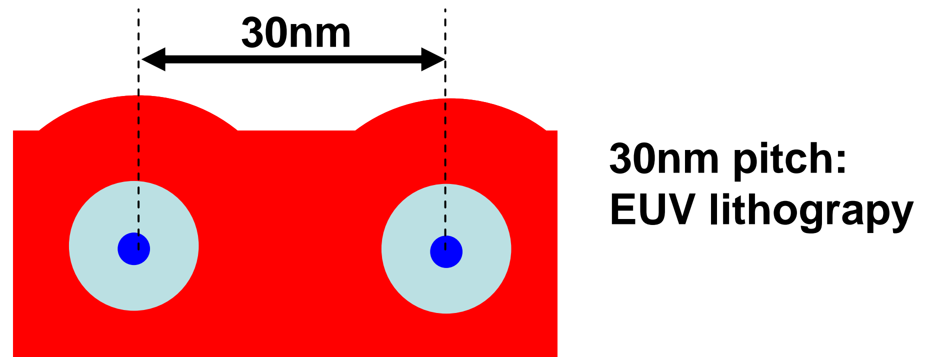
Front gate type MOS 165 wires /μm

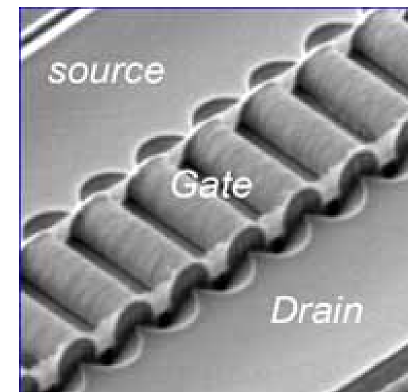


Surrounded gate type MOS 33 wires/μm



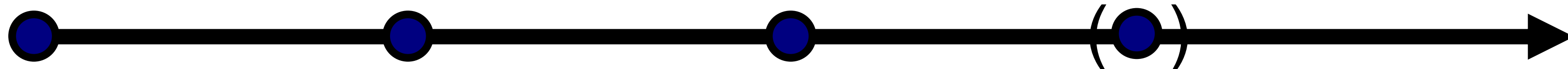






Surrounded gate MOS

Device fabrication

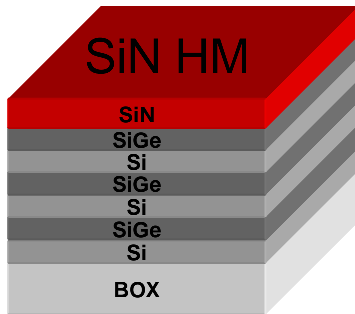


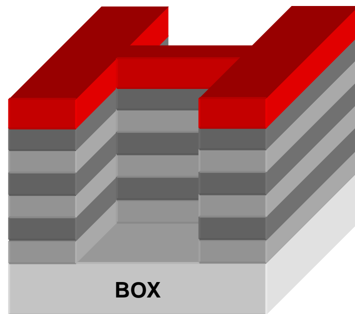
$Si/Si_{0.8}Ge_{0.2}$ superlattice epitaxy on SOI

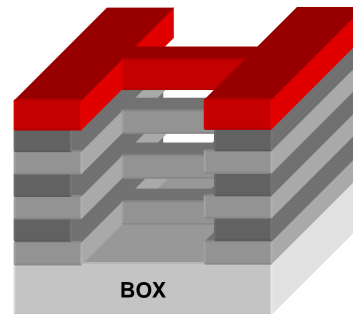
Anisotropic etching of these layers

Isotropic etching of SiGe

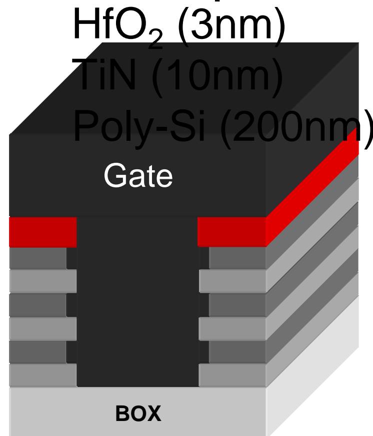
The NW diameter is controllable down to 5 nm by self limited oxidation.



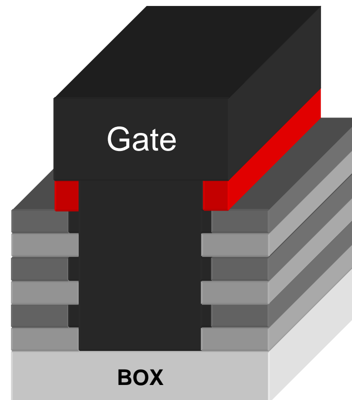




Gate depositions
HfO_2 (3nm)
TiN (10nm)
Poly-Si (200nm)



Gate etching

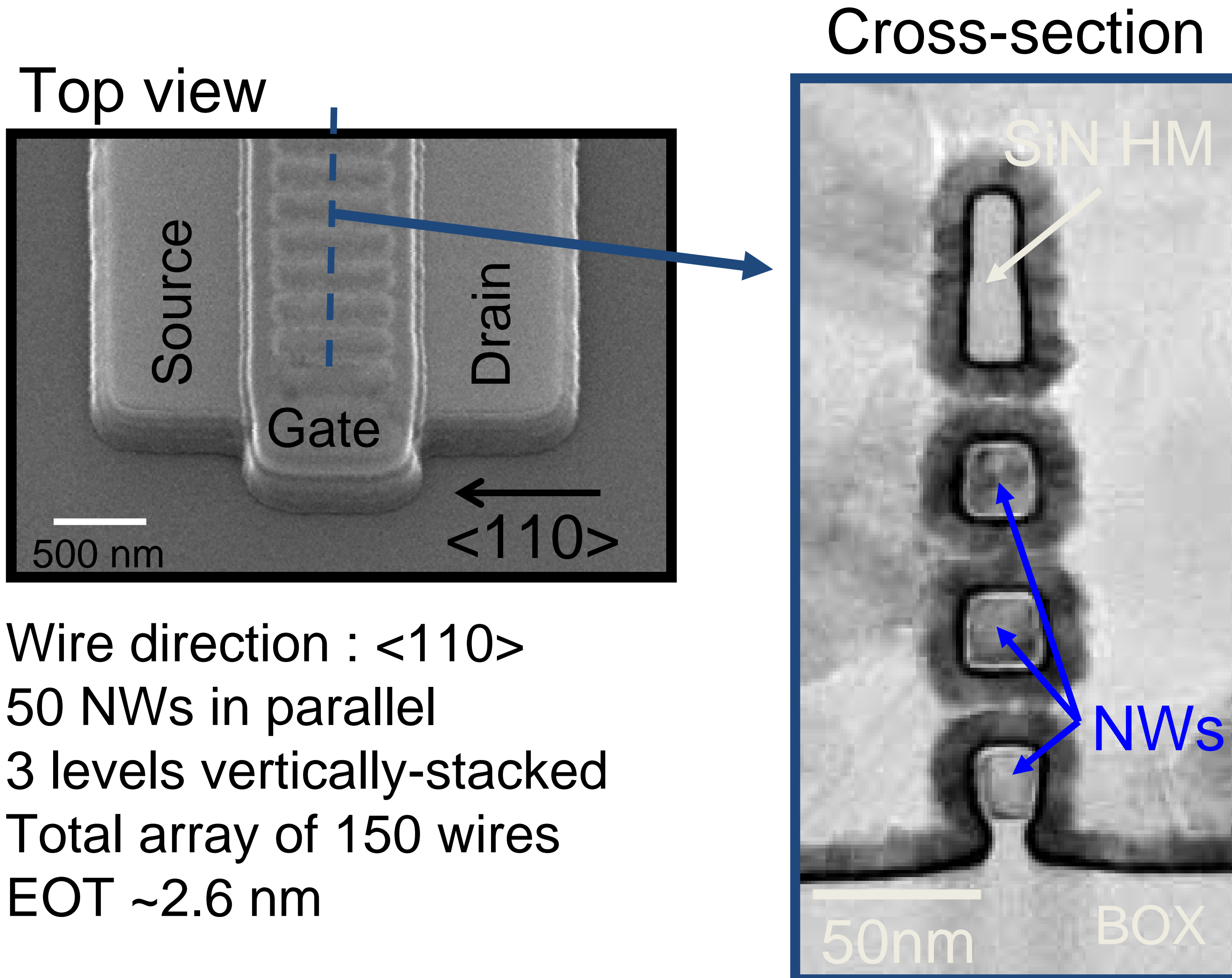


S/D implantation
Spacer formation
Activation anneal
Salicidation

Standard Back-End of-Line Process

Process Details :
C. Dupre *et al.*,
IEDM Tech. Dig., p.749, 2008

3D-stacked Si NWs with Hi-*k*/MG

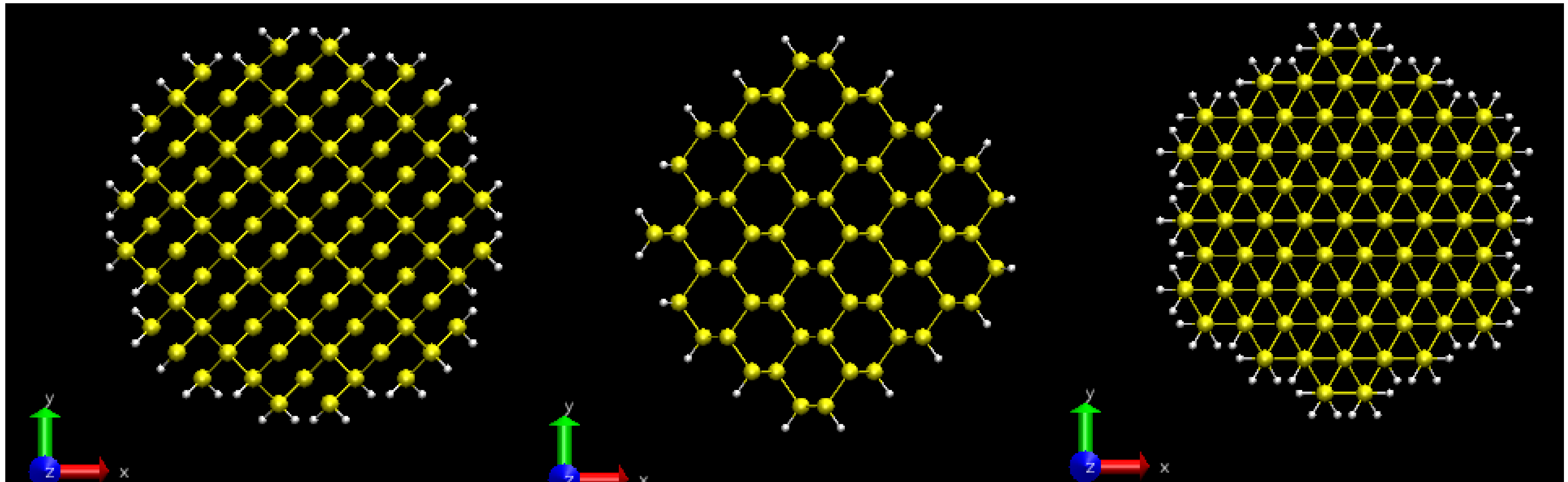


Wire direction : <110>
50 NWs in parallel
3 levels vertically-stacked
Total array of 150 wires
EOT ~2.6 nm

SiNW Band structure calculation

Cross section of Si NW

First principal calculation,

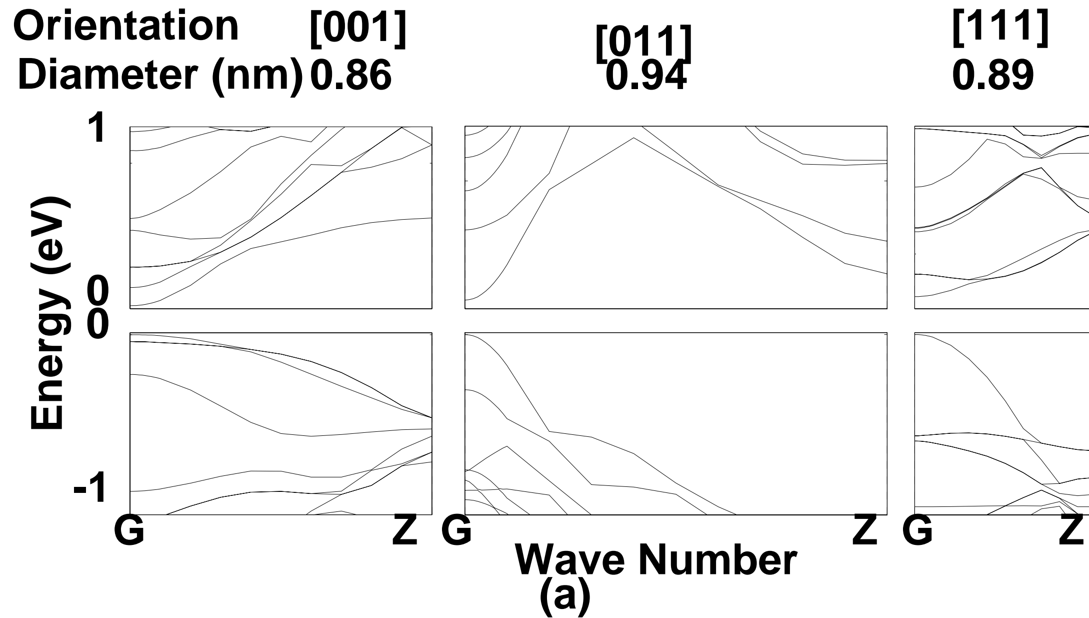


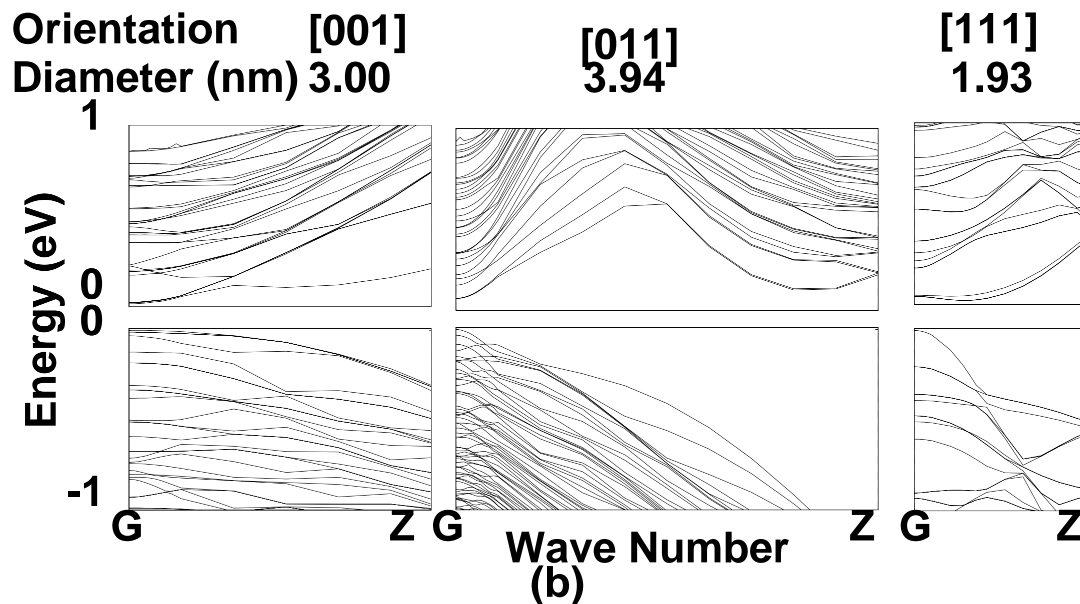
D=1.96nm
[001]

D=1.94nm
[011]

D=1.93nm
[111]

Si nanowire FET with 1D Transport

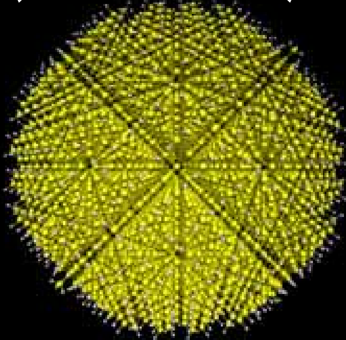


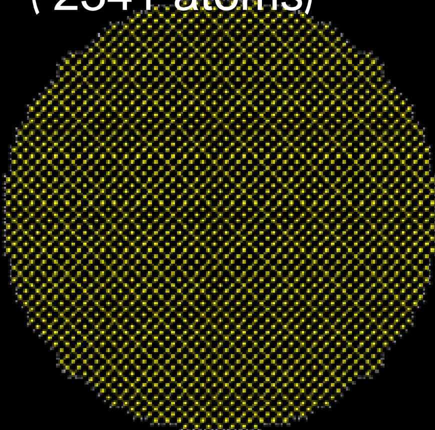


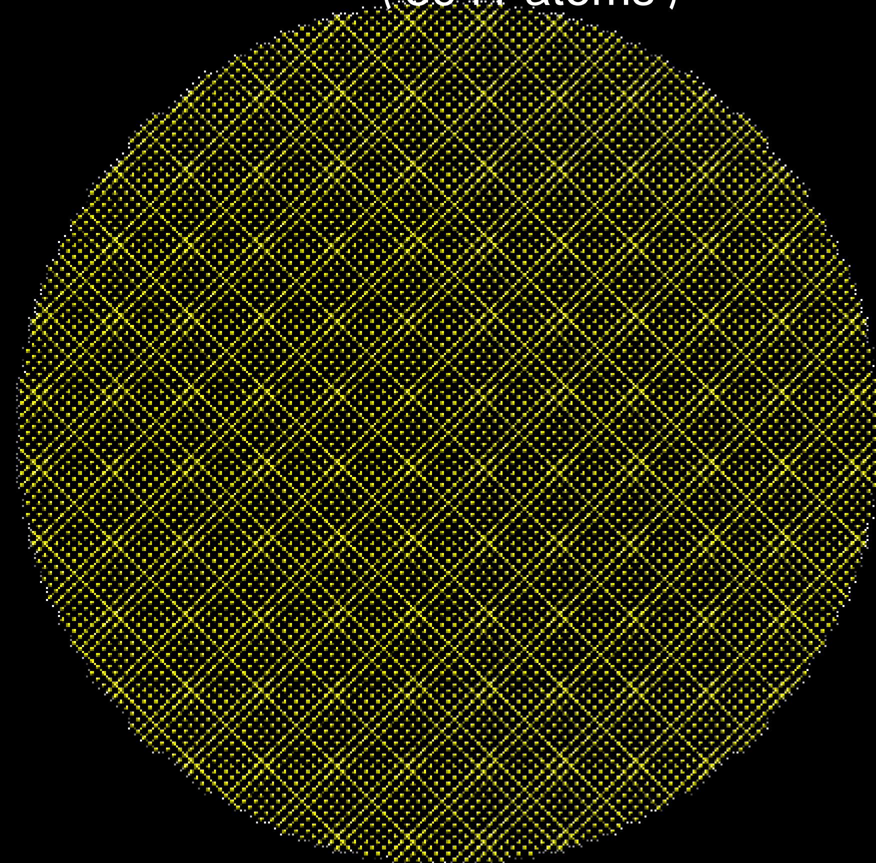
Small mass with [011]

Large number of quantum channels with [001]

Atomic models of a Si quantum dot and Si nanowires







RSDFT – suitable for parallel first-principles calculation -

- ✓Real-Space Finite-Difference
- ✓Sparse Matrix
- ✓FFT free (FFT is inevitable in the conventional plane-wave code)
- ✓MPI (Message Passing Interface) library

Higher-order finite difference pseudopotential method
J. R. Chelikowsky et al., Phys. Rev. B, (1994)

Kohn-Sham eq. (finite-difference)

$$\left(-\frac{1}{2}\nabla^2 + v_s[\rho](\mathbf{r}) + \hat{v}_{nloc}^{PP}(\mathbf{r})\right)\phi_n(\mathbf{r}) = \varepsilon_n \phi_n(\mathbf{r})$$

Higher-order finite difference

$$\frac{\partial^2}{\partial x^2}\psi_n(x,y,z) \approx \sum_{m=-6}^{6} C_m \psi_n(x+m\Delta x, y, z)$$

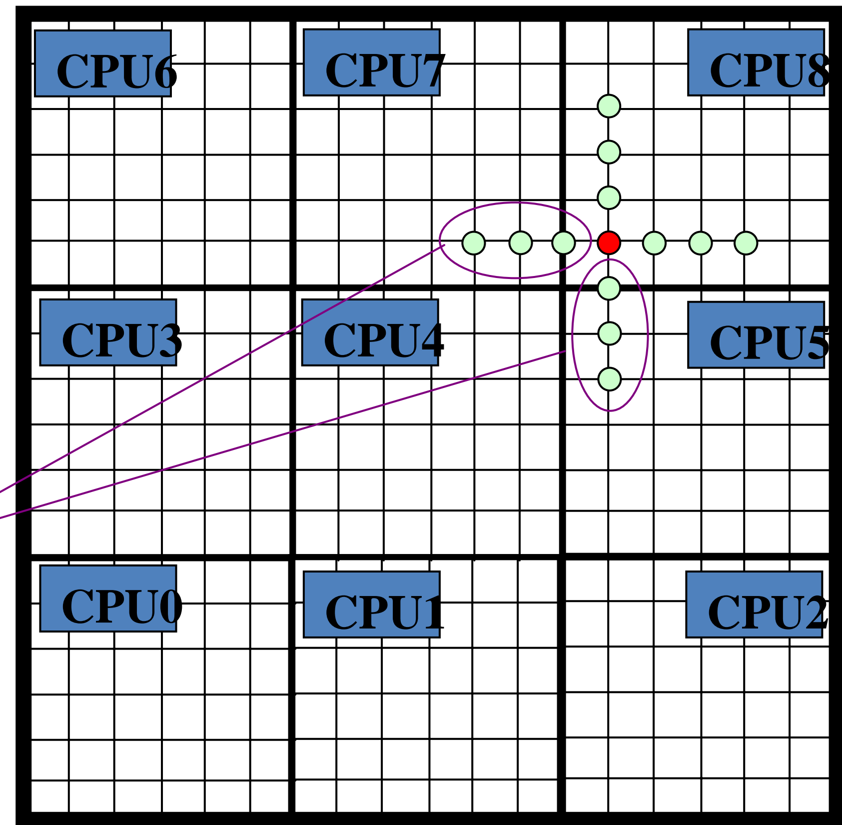
MPI_ISEND, MPI_IRECV

Integration

$$\int \psi_m(\mathbf{r})\psi_n(\mathbf{r})d\mathbf{r} \approx \sum_{i=1}^{Mesh} \psi_m(\mathbf{r}_i)\psi_n(\mathbf{r}_i)\Delta x \Delta y \Delta z$$

MPI_ALLREDUCE

3D grid is divided by several regions
for parallel computation.



Massively Parallel Computing

with our recently developed code “RSDFT”

Iwata et al, J. Comp. Phys., to be published

Real-Space Density-Functional Theory code (RSDFT)

Based on the finite-difference pseudopotential method (J. R. Chelikowsky et al., PRB1994)

Highly tuned for massively parallel computers

Computations are done on a massively-parallel cluster **PACS-CS** at University of Tsukuba.

(Theoretical Peak Performance = 5.6GFLOPS/node)

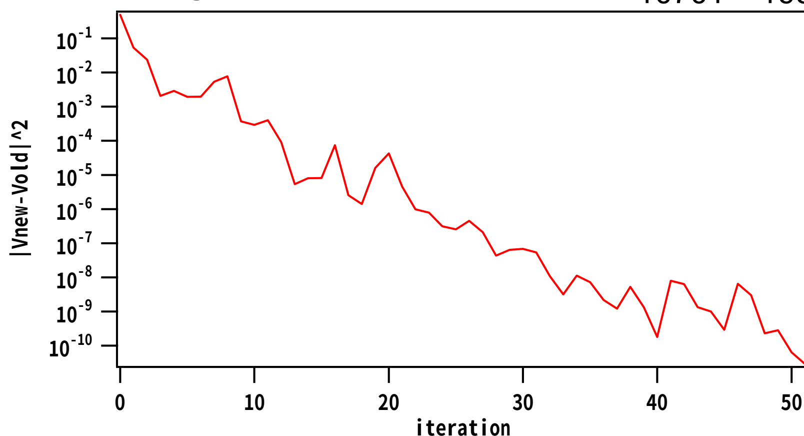
e.g.) The system over 10,000 atoms → $Si_{10701}H_{1996}$

(7.6 nm diameter Si dot)

Convergence behavior for $Si_{10701}H_{1996}$

Grid points = 3,402,059

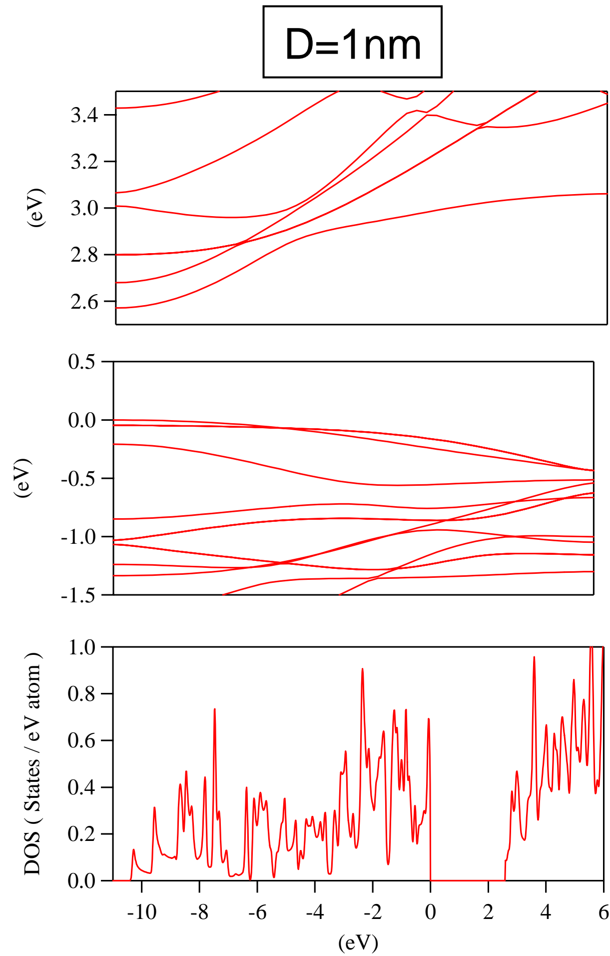
Bands = 22,432

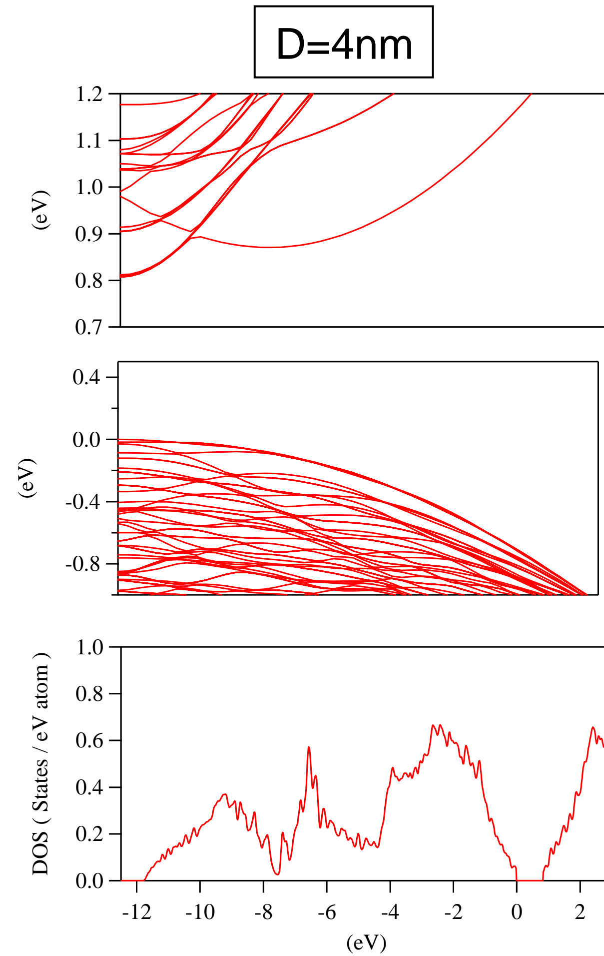


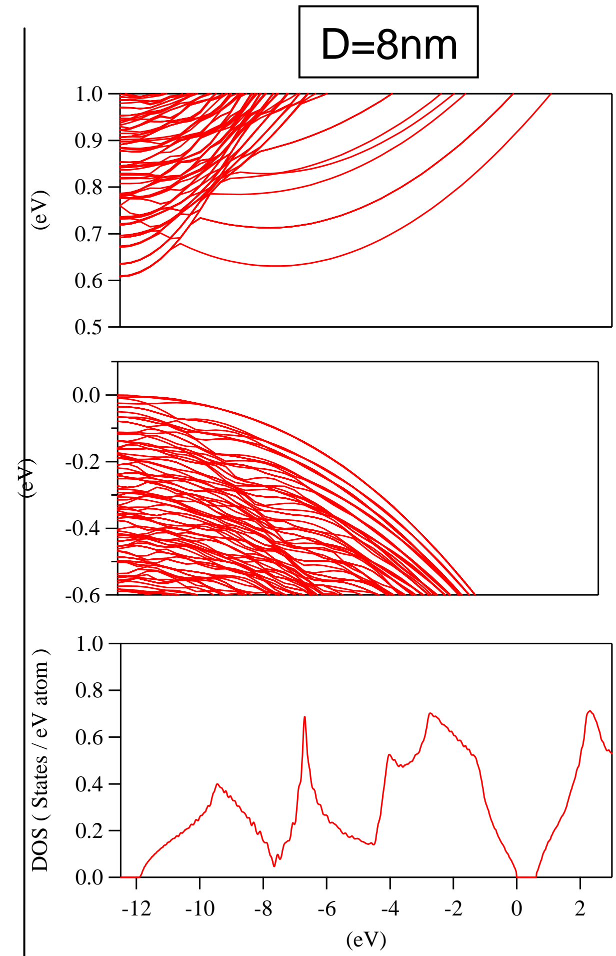
Computational Time (with 1024 nodes of PACS-CS

6781 sec. × 60 iteration step = 113 hour

Band Structure and DOS of Si(100)NWs (D=1nm, 4nm, and 8nm)







D=1 nm
Si21H20 (41 atoms)
KS band gap=2.60eV

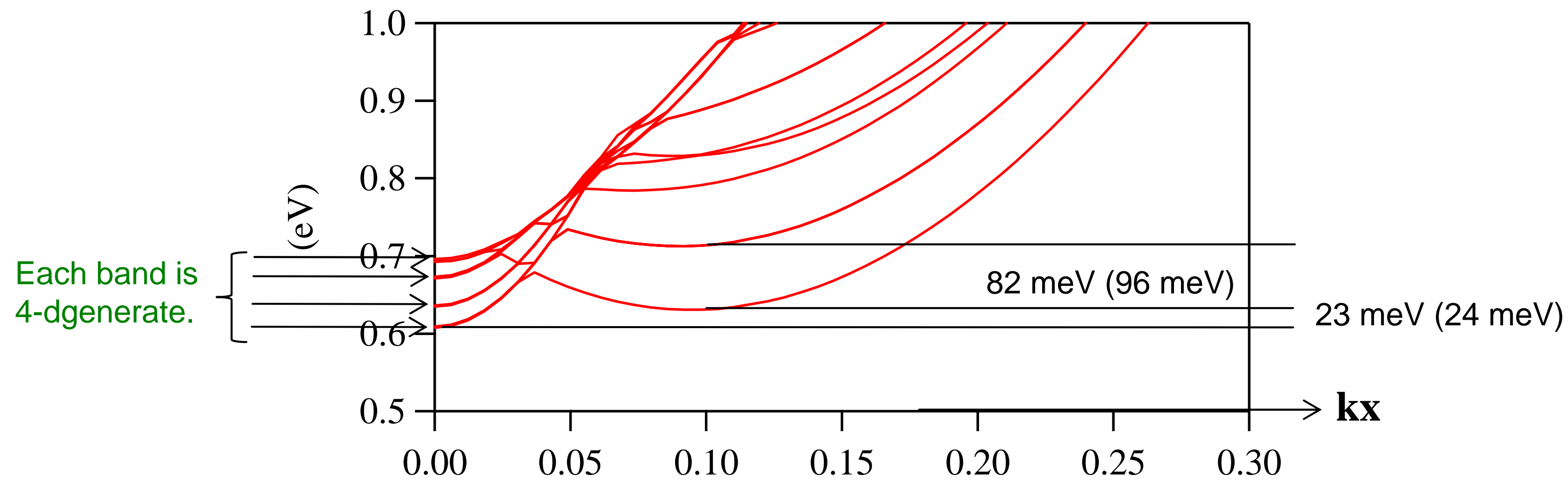
D = 4 nm
Si341H84 (425 atoms)
KS band gap = 0.81eV

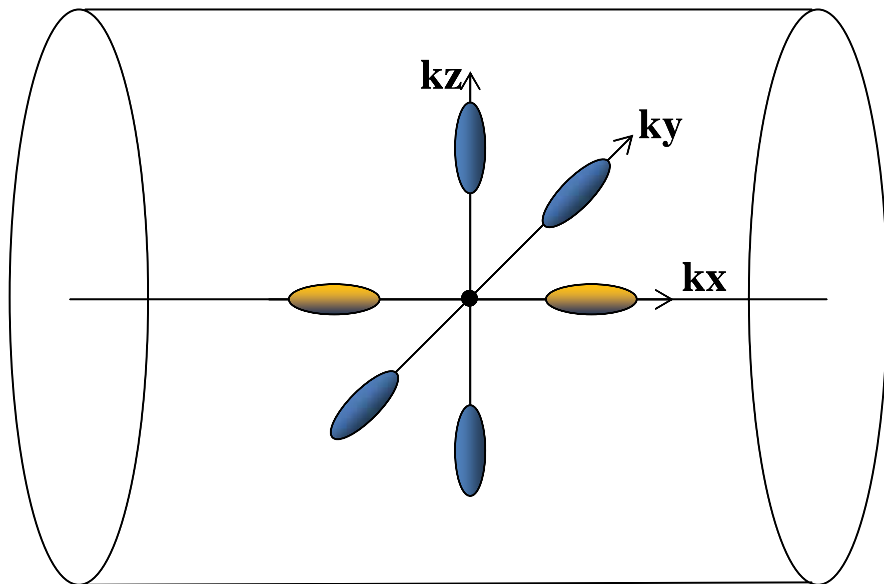
D=8 nm
Si1361H164 (1525 atoms)
KS band gap=0.61eV

KS band gap of bulk (LDA) = 0.53eV

Band structure of 8-nm-diameter Si nanowire near the CBM

- KS band gap = 0.608 eV (@Γ)



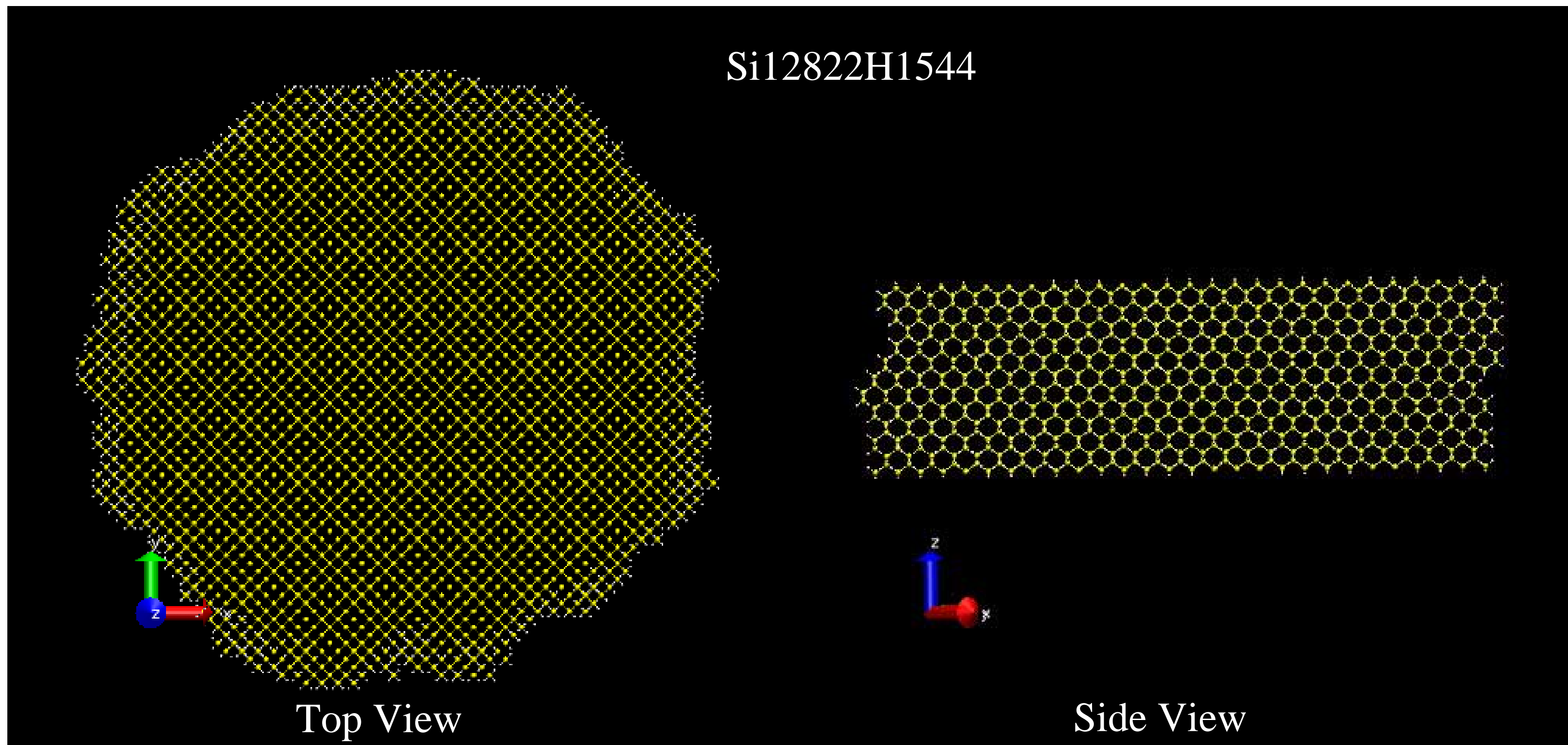


Effective mass equation

$$\left[-\frac{\hbar^2}{2m_t^*}\left(\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2}\right)-\frac{\hbar^2}{2m_l^*}\frac{\partial^2}{\partial z^2}\right]\Phi(\mathbf{r})=(\varepsilon-\varepsilon_{CBM})\Phi(\mathbf{r})$$

The band structure can be understood that electrons near the CBM in the bulk Si are Confined within a cylindrical geometry.

Si nano wire with surface roughness

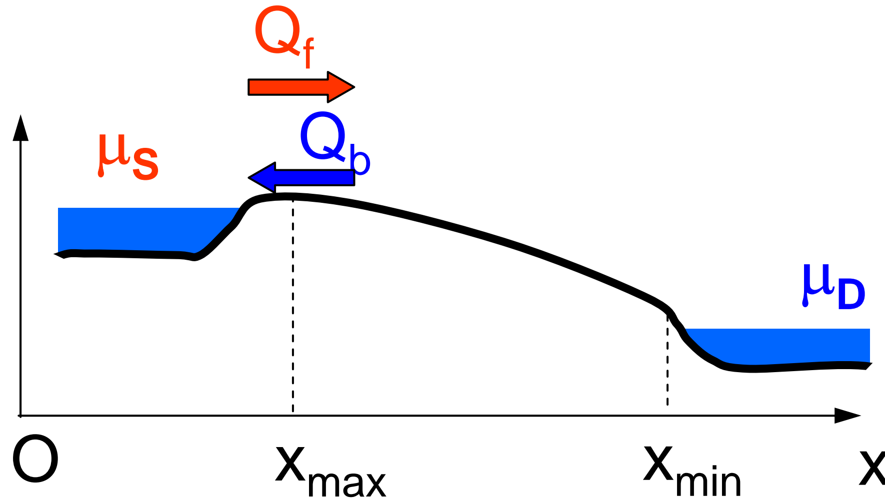


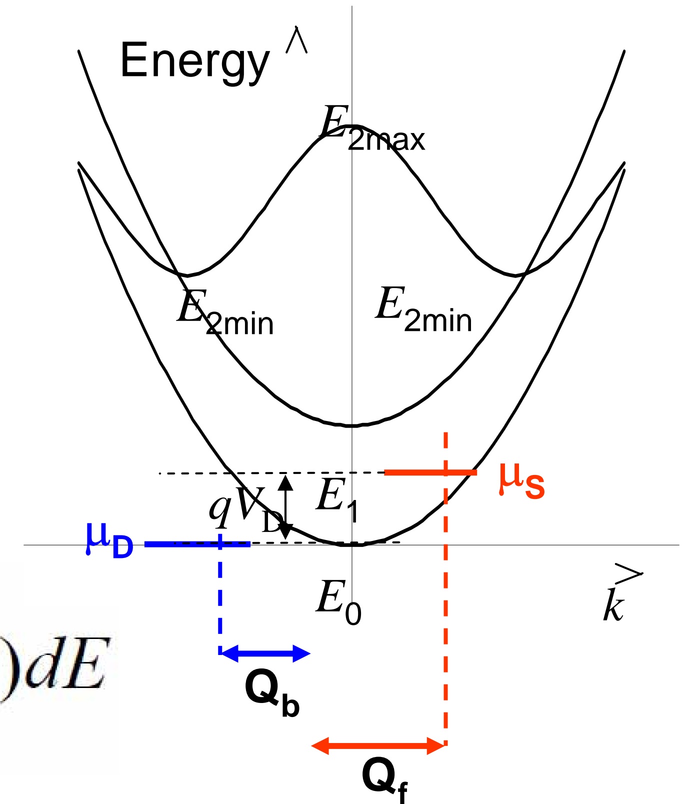
Si12822H1544 (14,366 atoms)

- 10nm diameter、3.3nm height、(100)
- Grid spacing：0.45Å (~14Ry)
- # of grid points：4,718,592
- # of bands：29,024
- Memory：1,022GB〜2,044GB

SiNW Band compact model

Landauer Formalism for Ballistic FET



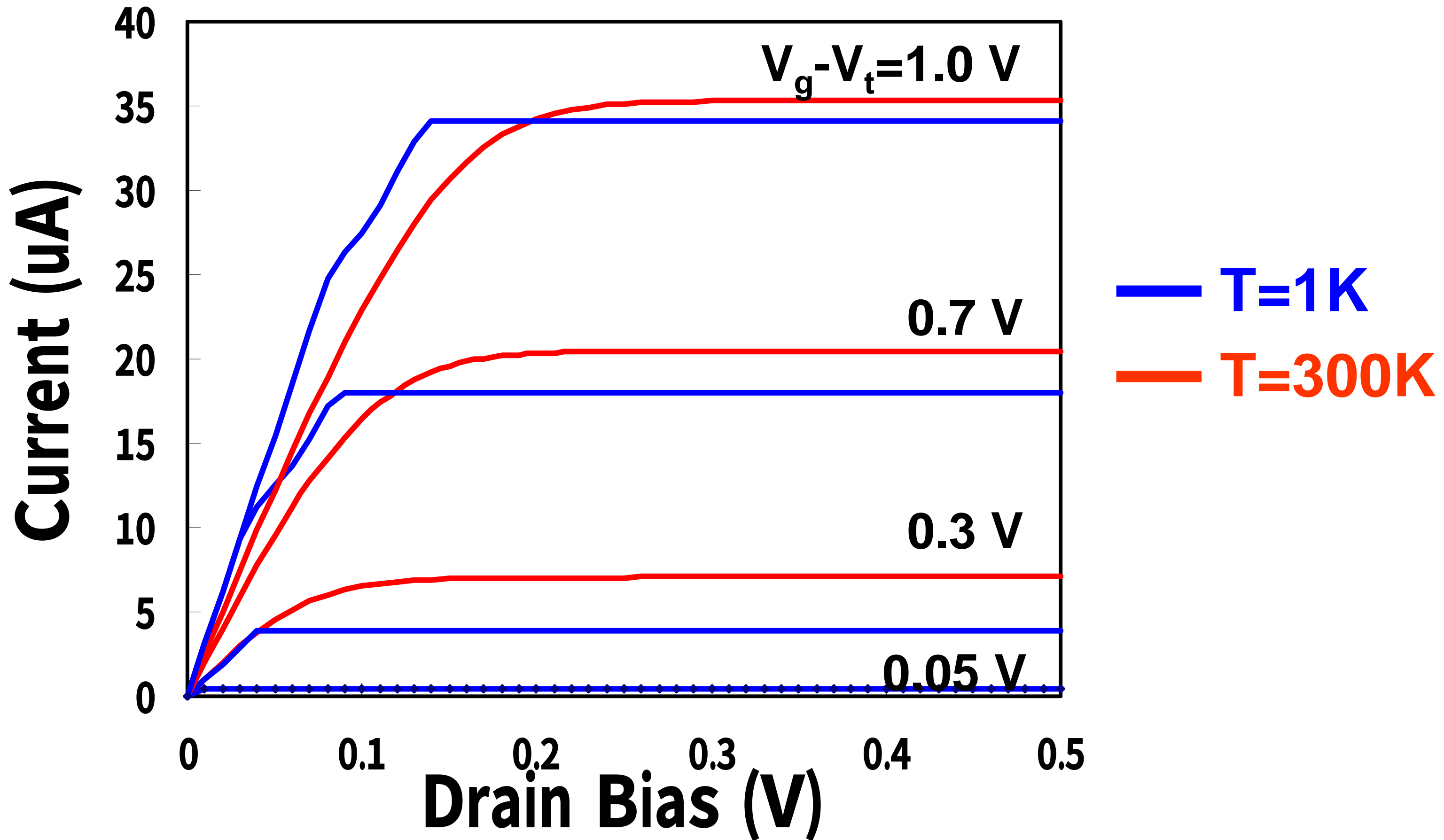


$$I_D = \frac{q}{\pi\hbar}\sum_i \int \left[f(E,\mu_S) - f(E,\mu_D)\right] T_i(E)\,dE$$

From x_{max} to x_{min} $\quad T_i(E) \approx 1$

$$I_D = G_0\left(\frac{k_B T}{q}\right)\sum_i g_i \ln\left\{\frac{1+\exp\left[(\mu_S - E_{i0})/k_B T\right]}{1+\exp\left[(\mu_D - E_{i0})/k_B T\right]}\right\}$$

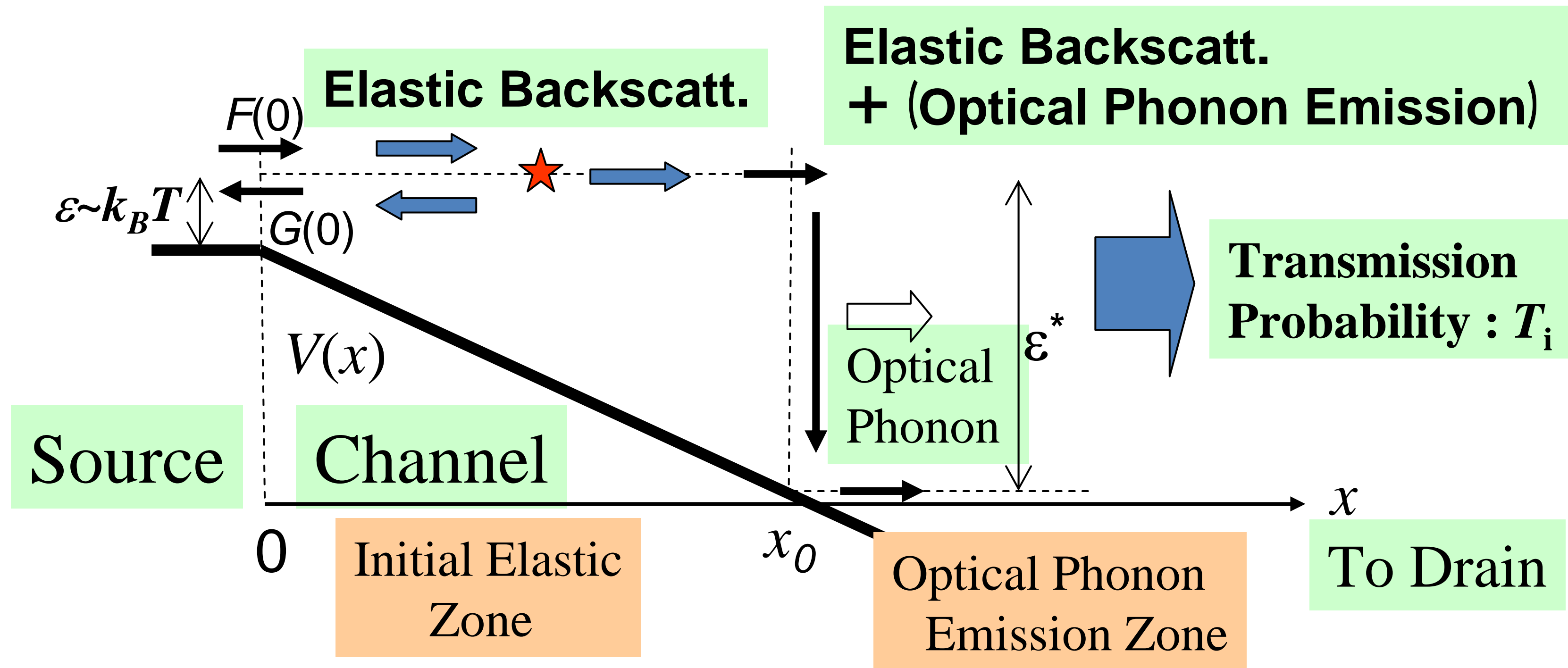
IV Characteristics of Ballistic SiNW FET



Small temperature dependency
35μA/wire for 4 quantum channels

Model of Carrier Scattering

Linear Potential Approx.： Electric Field E



Transmission Probability to Drain

$$T(\varepsilon) = \left. \frac{F(0) - G(0)}{F(0)} \right)_{\text{Injection from Drain}=0}$$

Résumé of the Compact Model

$$I = \frac{q}{\pi\hbar}\sum_i g_i \int \left[f(\varepsilon,\mu_s) - f(\varepsilon,\mu_D) \right] T_i \, d\varepsilon$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left\{\frac{\sqrt{2r+t_{ox}}+\sqrt{t_{ox}}}{\sqrt{2r+t_{ox}}-\sqrt{t_{ox}}}\right\}}.$$

Planar Gate

$$(V_G - V_t) - \alpha\frac{\mu_S-\mu_0}{q} = \frac{\left|Q_f+Q_b\right|}{C_G}.$$

$$\mu_S - \mu_D = qV_D$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left(\frac{r+t_{ox}}{r}\right)}.$$

GAA

(Electrostatics requirement)

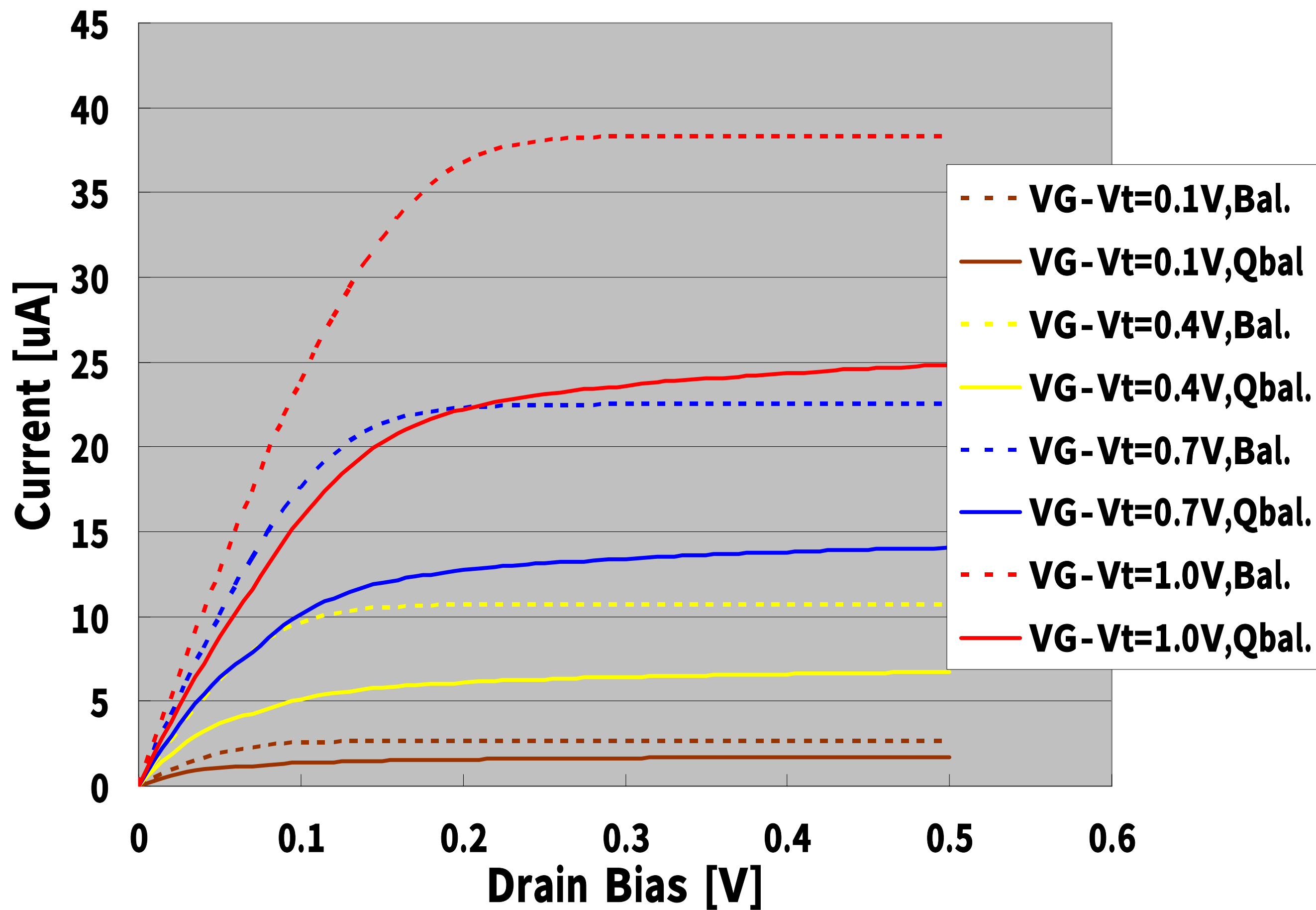
$$\left|Q_f+Q_b\right| = \frac{q}{\pi}\sum_i g_i \left[\int_{-\infty}^{\infty} \frac{dk}{1+\exp\left\{\frac{\varepsilon_i(k)-\mu_S}{k_BT}\right\}} - \int_{-\infty}^{0} \left\{ \frac{1}{1+\exp\left\{\frac{\varepsilon_i(k)-\mu_S}{k_BT}\right\}} - \frac{1}{1+\exp\left\{\frac{\varepsilon_i(k)-\mu_D}{k_BT}\right\}} \right\} T_i(\varepsilon_i(k))\,dk \right]$$

(Carrier distribution in Subbands)

$$T(\varepsilon) = \frac{\sqrt{2D_0}\,qE}{\left(\sqrt{B_0+D_0}+\sqrt{D_0}\right)qE + \sqrt{2mD_0}\,B_0 \ln\left(\frac{qEx_0+\varepsilon}{\varepsilon}\right)}$$

Unknowns are I_D, $(\mu_S-\mu_0)$, $(\mu_D-\mu_0)$, (Q_f+Q_b)

I-V_D Characteritics (RT)

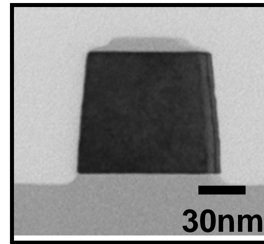


- Electric current 20～25 μA
- No satruration at Large V_D

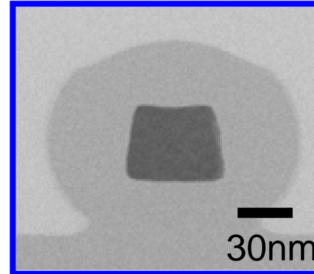
SiNW FET Fabrication

SiNW FET Fabrication

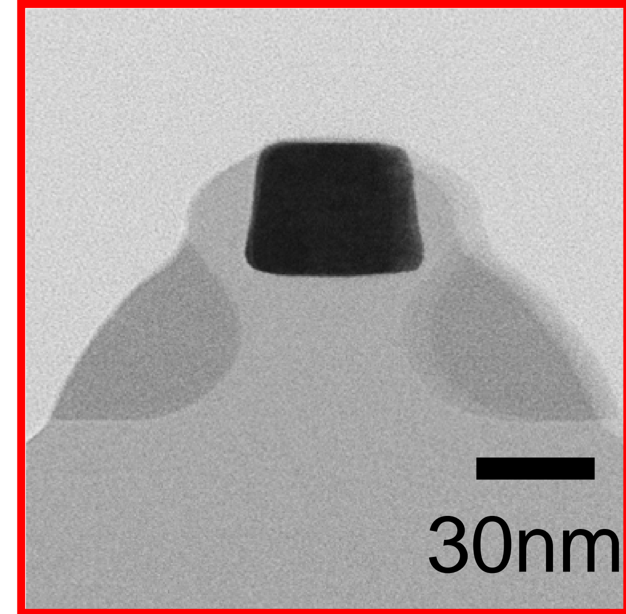
- S/D & Fin Patterning



- Sacrificial Oxidation



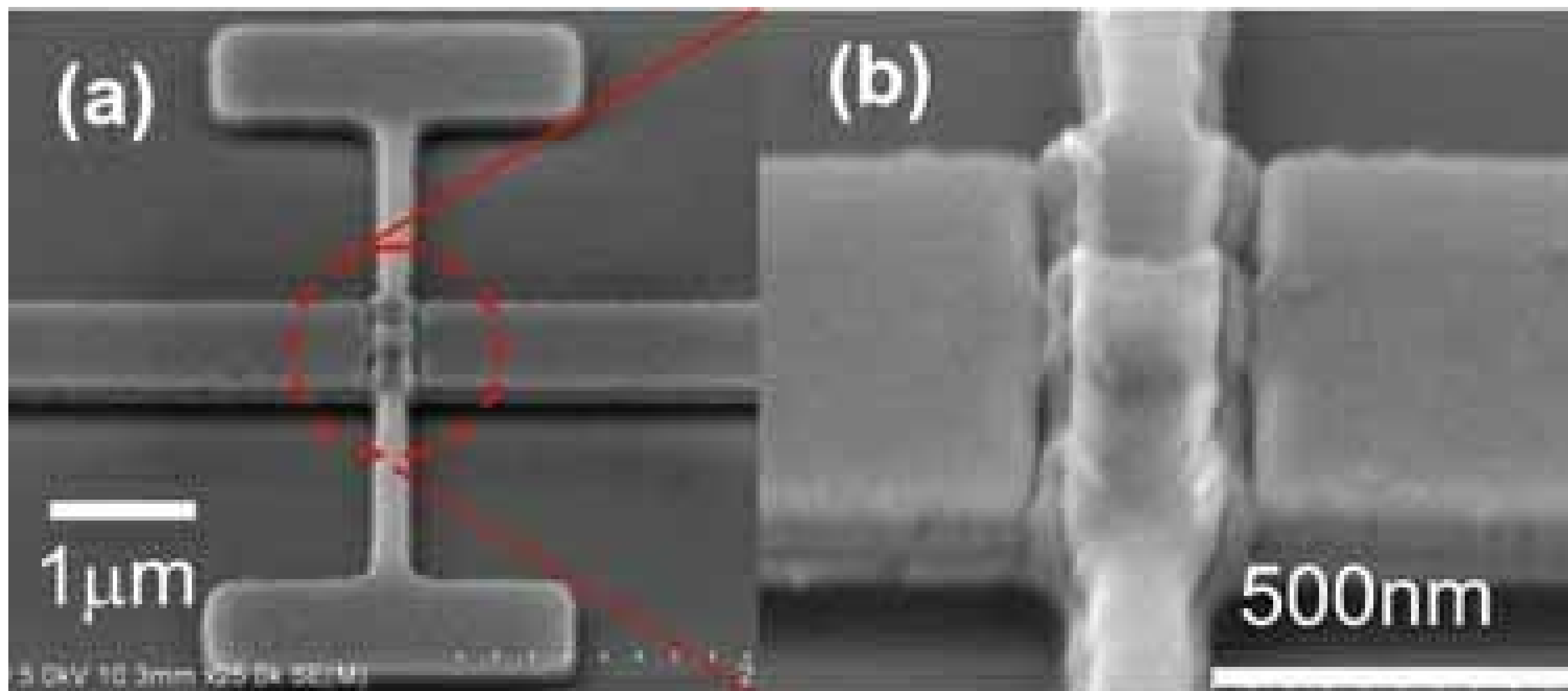
- Oixde etch back
- SiN sidewall support formation



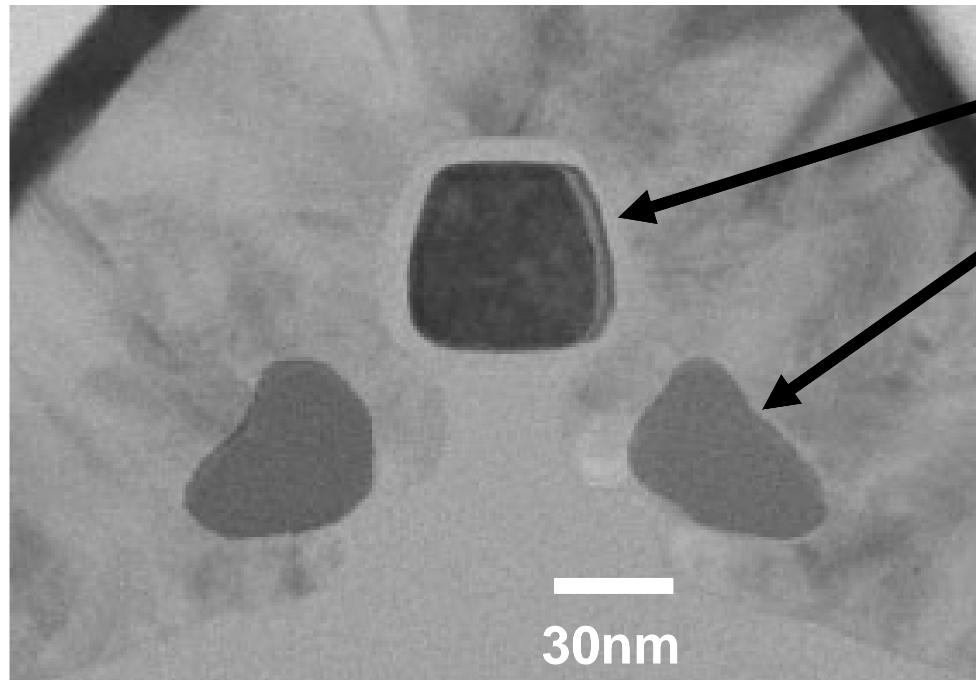
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)
- Backend

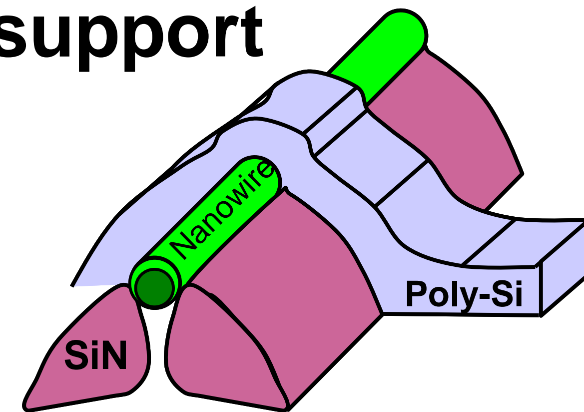
Standard recipe for gate stack formation

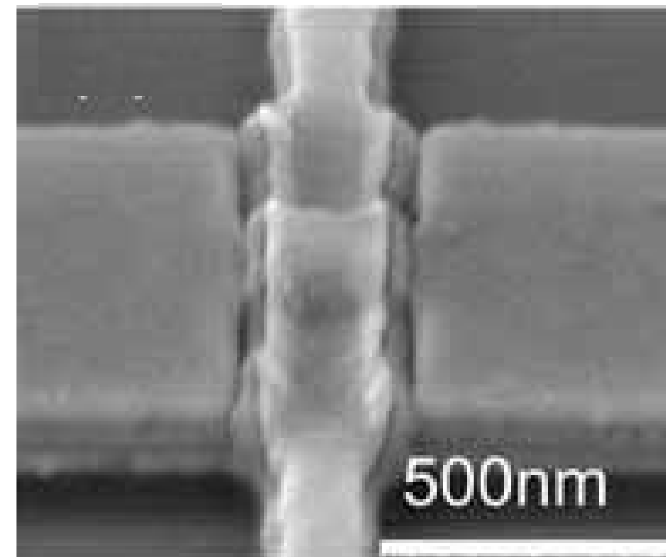
(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.



Fabricated SiNW FET

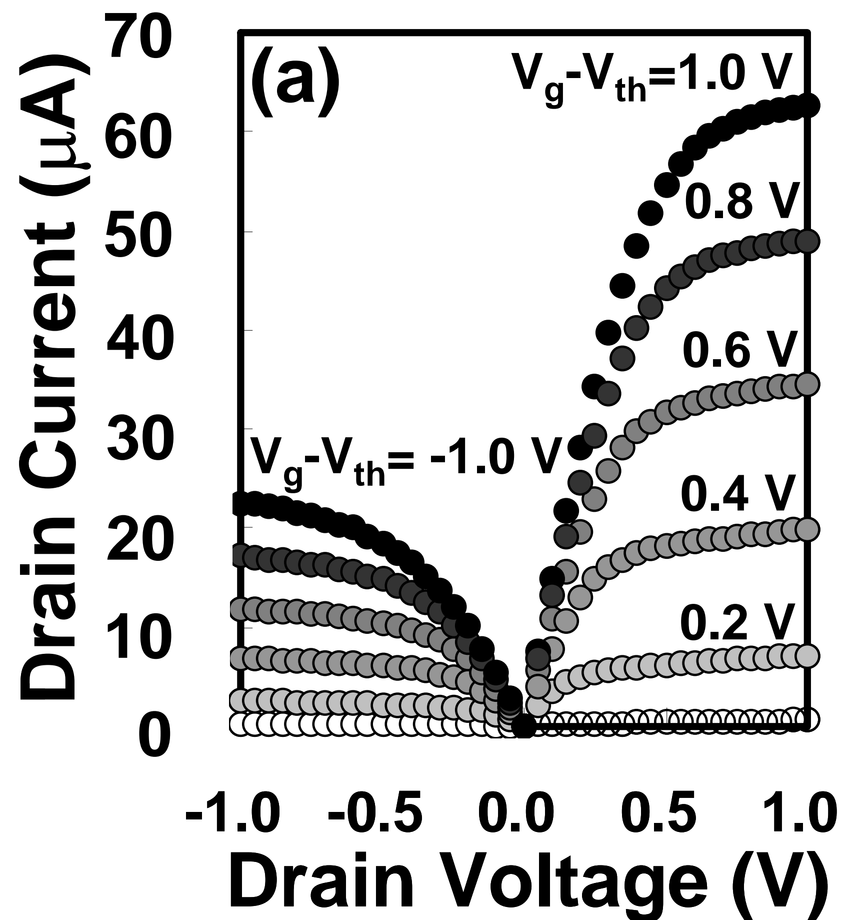


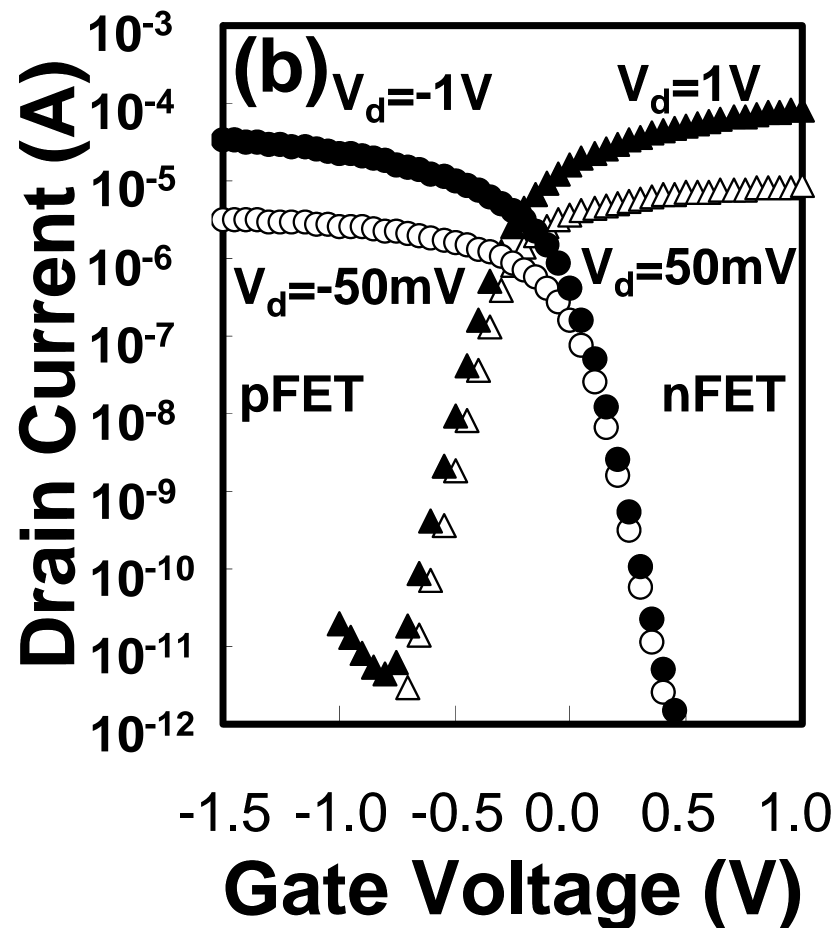




Recent results to be presented by ESSDERC 2010 next week in Sevile

Wire cross-section: 20 nm X 10 nm

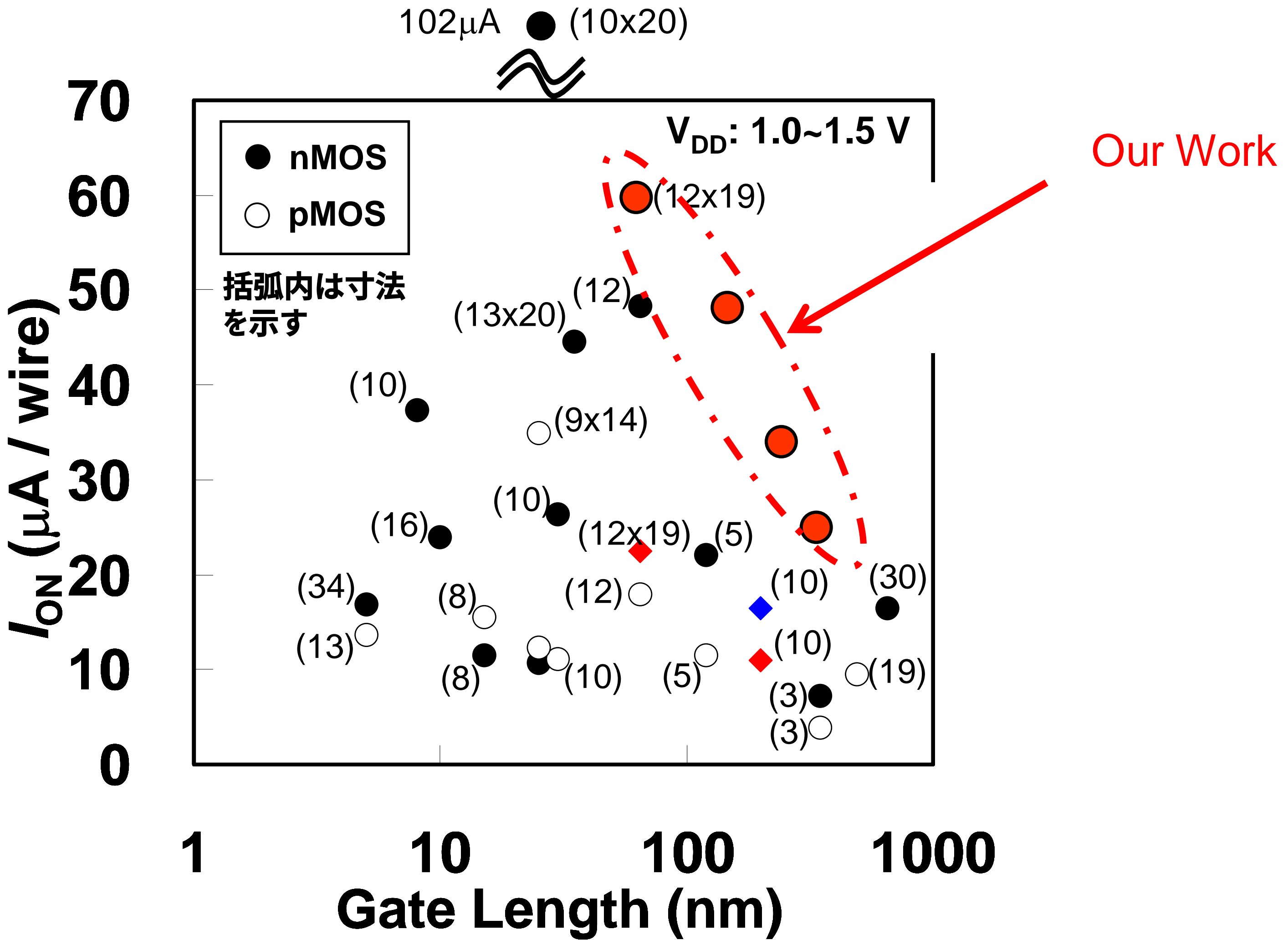




On/Off>10^6、60uA/wire

L_g=65nm, T_{ox}=3nm

Bench Mark



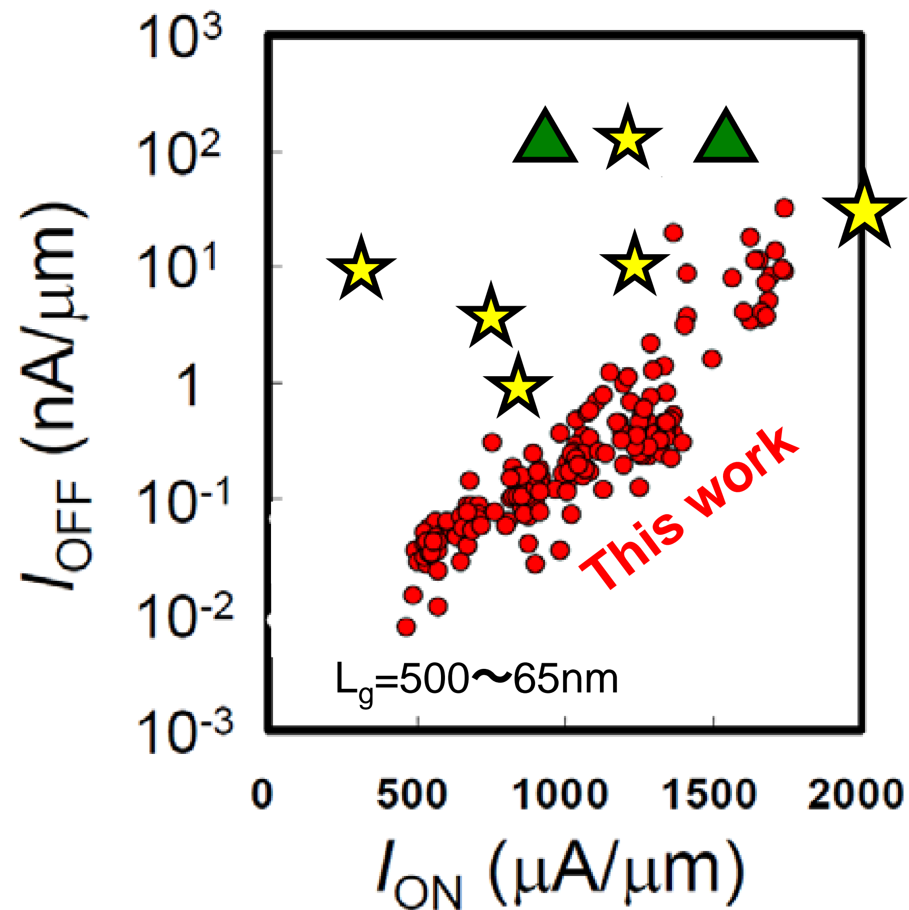
Bench Mark

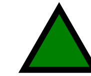
	This work	Ref[11]	Ref[12]	Ref[13]	Ref[14]	Ref[15]	Ref[4]
NW Cross-section (nm)	Rect.	Rect.	Rect.	Cir.	Cir.	Elliptical	Elliptical
NW Size (nm)	10x20	10x20	14	10	10	12	13x20
Lg (nm)	65	25	100	30	8	65	35
EOT or Tox (nm)	3	1.8	1.8	2	4	3	1.5
Vdd (V)	1.0	1.1	1.2	1.0	1.2	1.2	1.0
Ion(uA) per wire	60.1	102	30.3	26.4	37.4	48.4	43.8
Ion(uA/um) by dia.	3117	5010	2170	2640	3740	4030	2592
Ion(uA/um) by cir.	1609	2054	430	841	1191	1283	825
SS (mV/dec.)	70	79	68	71	75	~75	85
DIBL (mV/V)	62	56	15	13	22	40-82	65
Ion/Ioff	~1E6	>1E6	>1E5	~1E6	>1E7	>1E7	~2E5

Ref[11] by Stmicro Lg=25nm,Tox=1.8nm

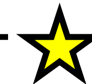
This work Lg=65nm,Tox=3nm

I_{ON}/I_{OFF} Bench mark

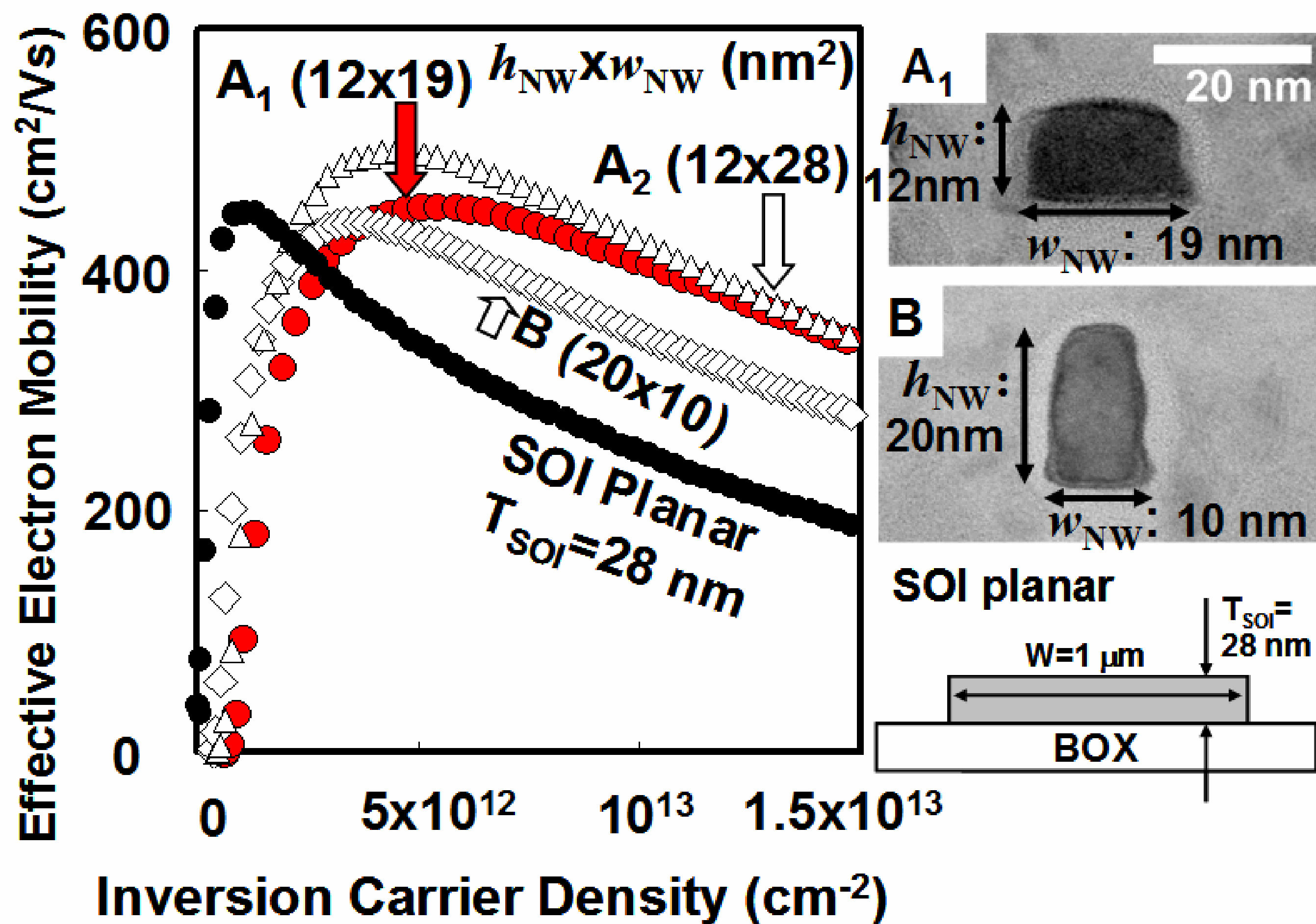


Planer FET  1.0〜1.1V

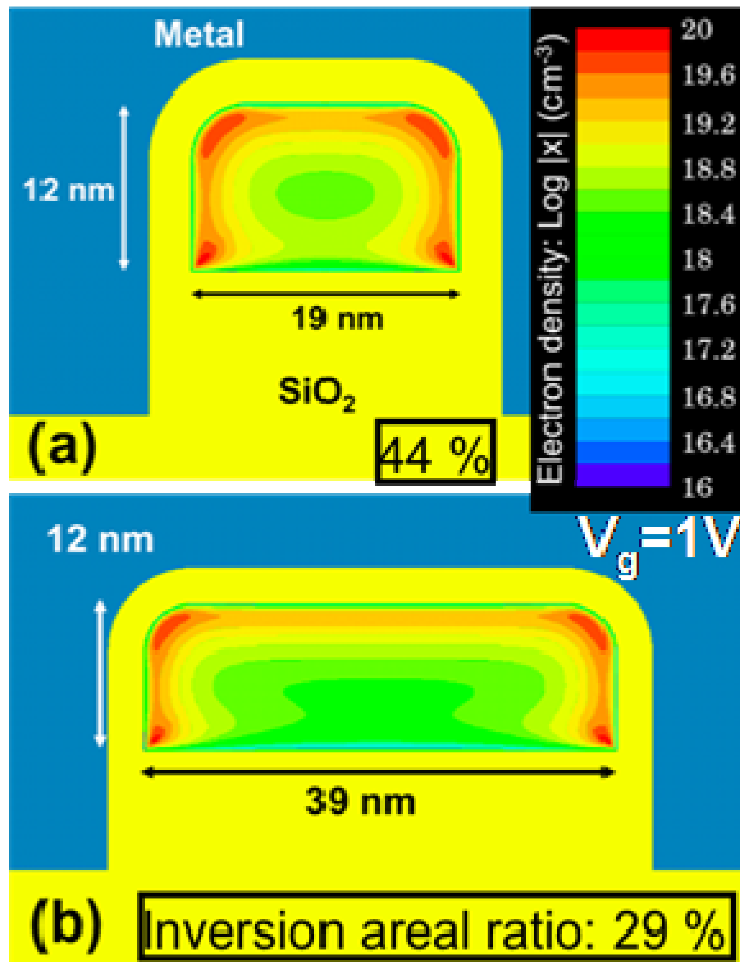
S. Kamiyama, IEDM 2009, p. 431
P. Packan, IEDM 2009, p.659

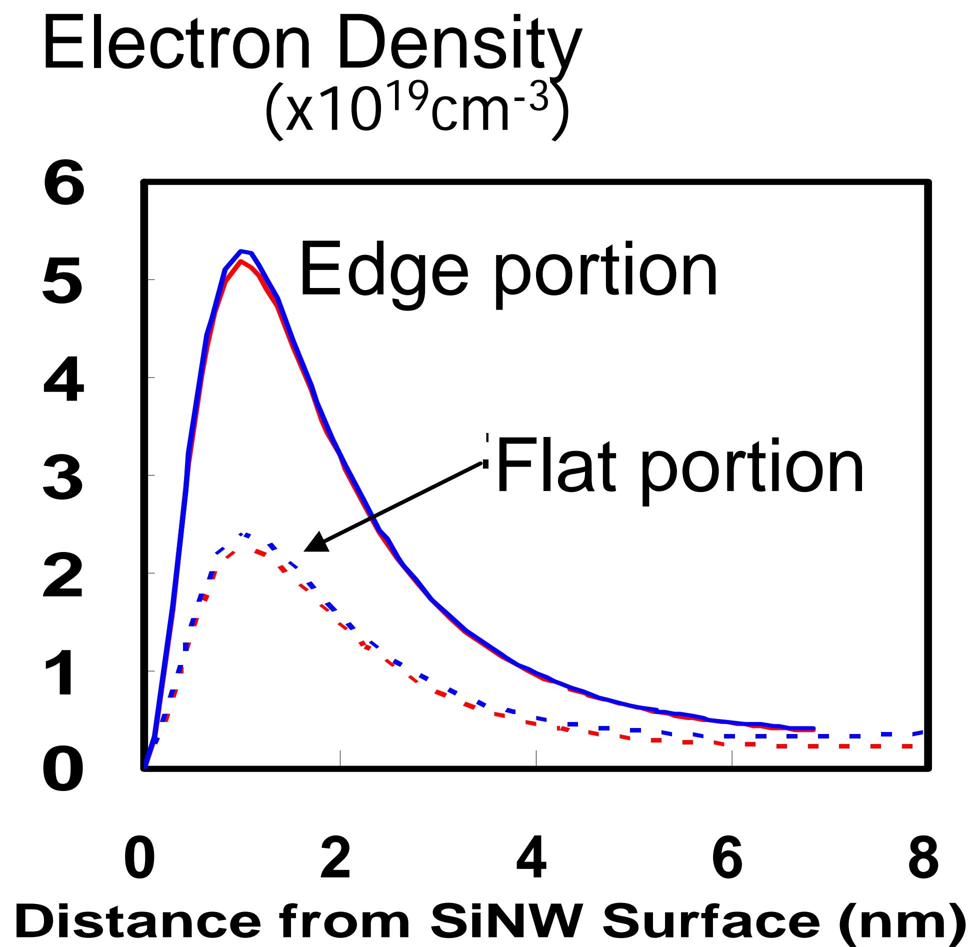
SiナノワイヤFET  1.2〜1.3V

Y. Jiang, VLSI 2008, p.34
H.-S. Wong, VLSI 2009, p.92
S. Bangsaruntip, IEDM 2009, p.297
C. Dupre, IEDM 2008, p. 749
S.D.Suk, IEDM 2005, p.735
G.Bidel, VLSI 2009, p.240

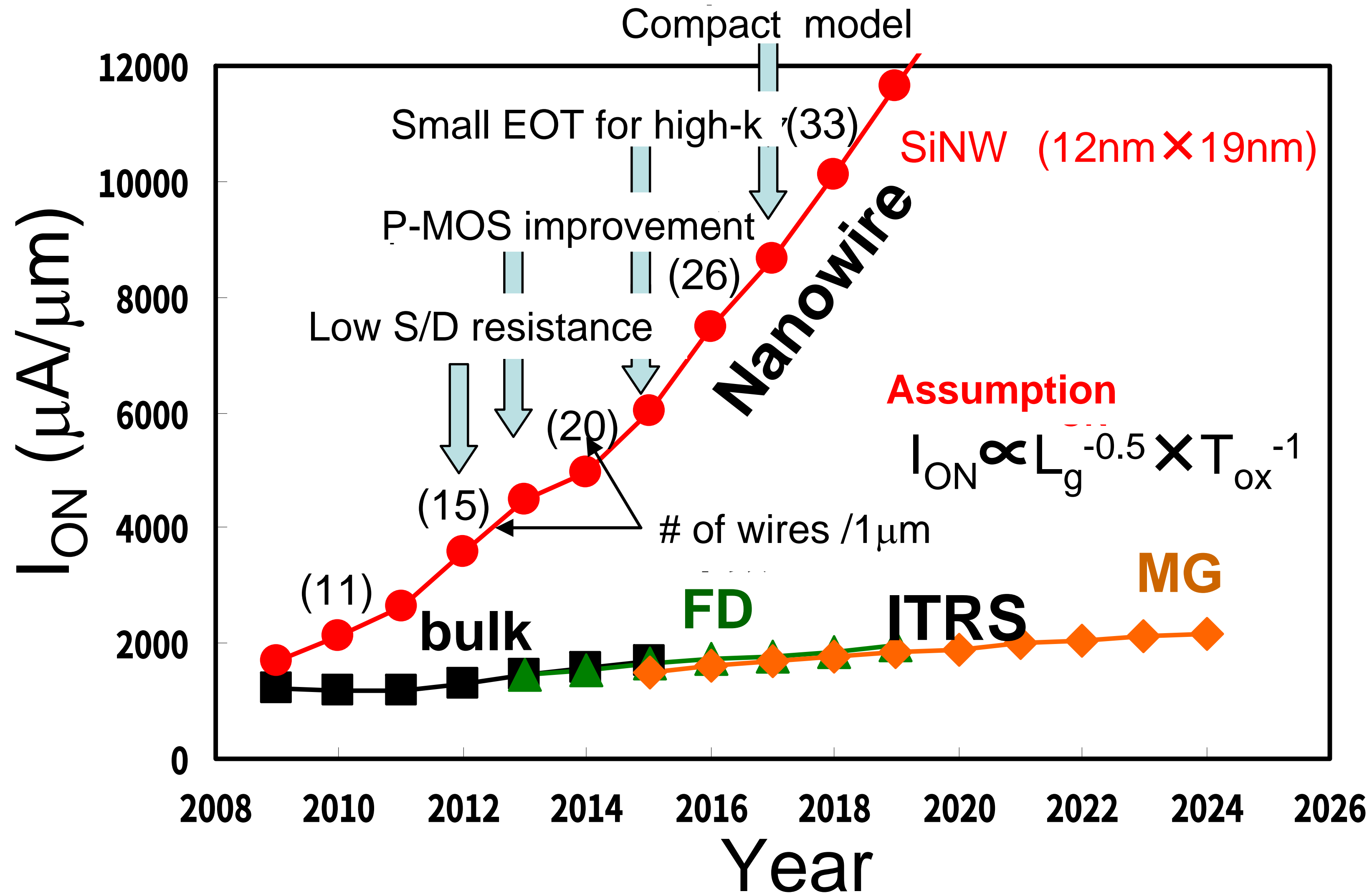


Effective Electron Mobility (cm²/Vs)
600
400
200
0
0
5x10¹²
10¹³
1.5x10¹³
Inversion Carrier Density (cm⁻²)
A1 (12x19)
hNWxwNW (nm²)
A2 (12x28)
B (20x10)
SOI Planar
TSOI=28 nm
A1
20 nm
hNW: 12nm
wNW: 19 nm
B
hNW: 20nm
wNW: 10 nm
SOI planar
TSOI= 28 nm
W=1 μm
BOX


Metal
12 nm
19 nm
SiO2
(a)
44 %
Electron density: Log |x| (cm-3)
20
19.6
19.2
18.8
18.4
18
17.6
17.2
16.8
16.4
16
Vg=1V
12 nm
39 nm
(b)
Inversion areal ratio: 29 %

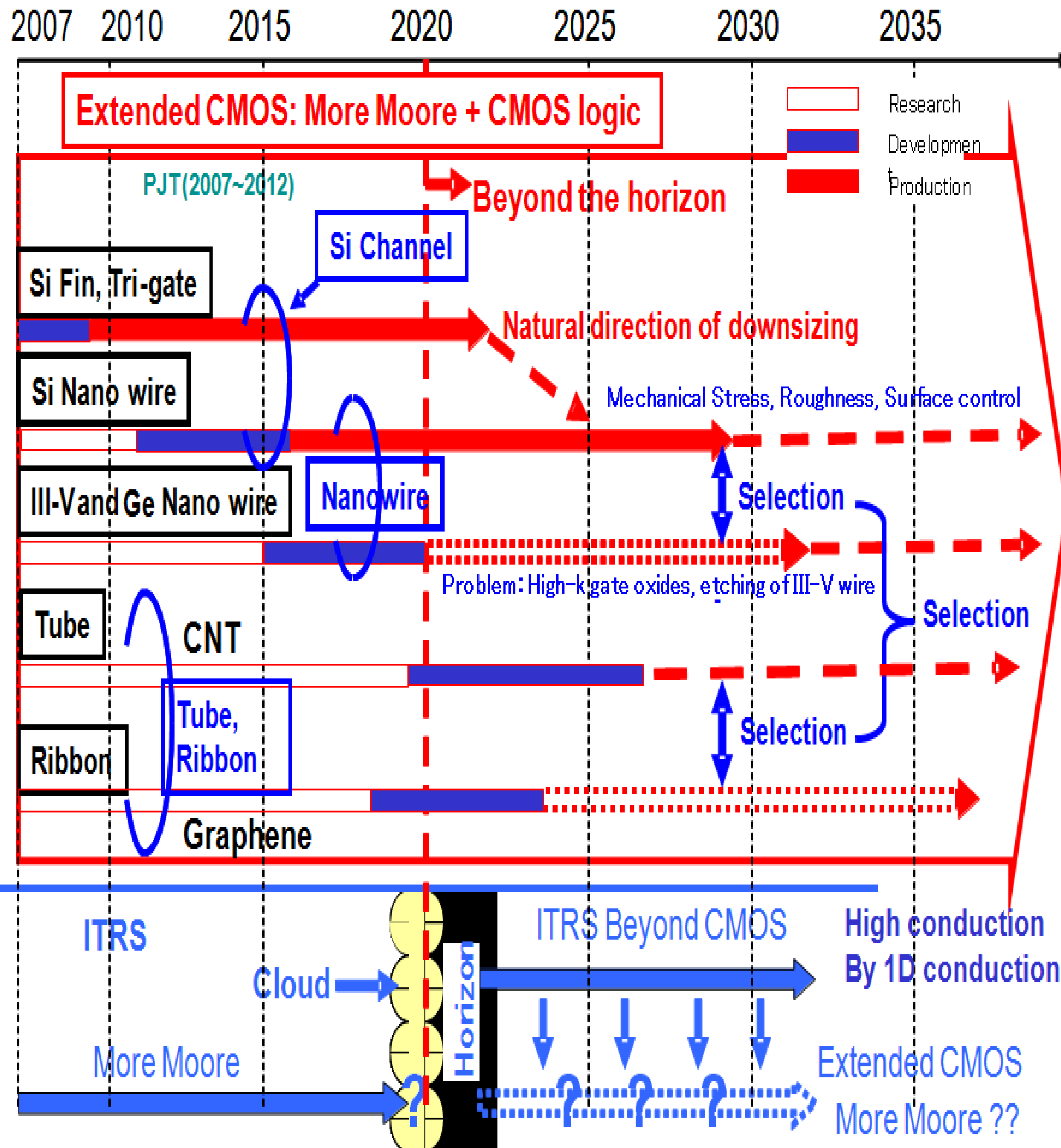

Electron Density
(x10^19cm^-3)
6
5
4
3
2
1
0
Edge portion
Flat portion
0
2
4
6
8
Distance from SiNW Surface (nm)

Primitive estimation !



Our roadmap for R &D

Source: H. Iwai, IWJT 2008



Current Issues

Si Nanowire

Control of wire surface property
Source Drain contact
Optimization of wire diameter
Compact I-V model

III-V & Ge Nanowire

High-k gate insulator
Wire formation technique

CNT:

Growth and integration of CNT
Width and Chirality control
Chirality determines conduction types: metal or semiconductor

Graphene:

Graphene formation technique
Suppression of off-current

Very small bandgap or no bandgap (semi-metal)

Control of ribbon edge structure which affects bandgap

Thank you for your attention